

AF 444 2123
Attorney Packet: 0325.00239

IN RE APPLICATION OF: Risto D. Bell et al.

SERIAL NO.: 09/410,160

TITLE: METHOD AND APPARATUS FOR AUTOMATED ENUMERATION, SIMULATION, IDENTIFICATION AND/OR IRRADIATION OF DEVICE ATTRIBUTES

FILED: September 30, 1999

EXAMINER: Garcia Otero, E.

ART UNIT: 2123

MAIL STOP APPEAL BRIEF - PATENTS
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| Independent Claims | 3 minus | 3 = | 0 x \$ 84.00 | \$ 0.00 |
| Multiple Dependent Claim First Added | | | + \$280.00 | \$ 0.00 |

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I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on June 9, 2003.

By:

Mary Donna Berkley
Mary Donna Berkley



Our Docket No.: 0325.00239

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#12

In re Application of:

Applicant: Risto D. Bell et al.

Application No.: 09/410,160

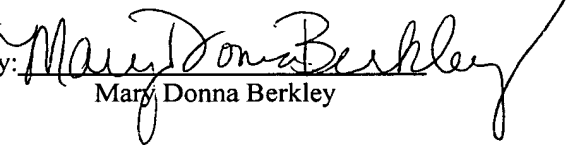
Examiner: Garcia Otero, E.

Filed: September 30, 1999

Art Group: 2123

For: METHOD AND APPARATUS FOR AUTOMATED ENUMERATION,
SIMULATION, IDENTIFICATION AND/OR IRRADIATION OF DEVICE
ATTRIBUTES

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on June 9, 2003.

By: 
Mary Donna Berkley

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
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Technology Center 2100

Dear Sir:

Appellants submit, in triplicate, the following Appeal Brief pursuant to 37 C.F.R. §1.192 for consideration by the Board of Patent Appeals and Interferences. Appellants also submit herewith a PTO-2038 Form in the amount of \$320.00 to cover the cost of filing the opening brief as required by 37 C.F.R. §1.17(f). Please charge any additional fees or credit any overpayment to our Deposit Account Number 50-0541.

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I. REAL PARTY IN INTEREST

The real party in interest is the Assignee, Cypress Semiconductor Corporation.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the Appellants, Appellants' legal representative, or Assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-20 are pending and remain rejected. The Appellants hereby appeal the rejections of claims 1-20.

IV. STATUS OF AMENDMENTS

Appellants are appealing a final Office Action issued by the Examiner on January 10, 2003. On February 26, 2003, Appellants filed a response requesting reconsideration. On March 24, 2003, the Examiner issued an Advisory Action that withdrew the 35 U.S.C. §112 rejections for claims 10, 18 and 19. On April 10, 2003, Appellants filed a Notice Of Appeal.

V. SUMMARY OF INVENTION

The present invention concerns a method of verifying a repair of a design (102). The method generally comprising the steps of (A) generating an enumeration of a plurality of fuses (108) in the design, (B) compiling data for each of the fuses (120), wherein the data comprises simulation

path data (118) and (C) simulating the design (106) with at least one of the fuses programmed for the repair to verify the repair.

VI. ISSUES

The issues are whether (i) claims 1 and 7 are patentable under 35 U.S.C. §112, first paragraph and (ii) claim 7 is patentable under 35 U.S.C. §112, second paragraph.

The issues are whether (i) claims 1, 3, 5-7, 12-16, 18 and 19 are patentable under 35 U.S.C. §103 over the Background of the Invention section of the instant application in view of Kablanian et al., U.S. Patent No. 5,764,878, (ii) claims 2 and 17 are patentable under 35 U.S.C. §103 over the Background of the Invention section in view of Kablanian et al. and Tzori, U.S. Patent No. 6,202,044, (iii) claim 4 is patentable under 35 U.S.C. §103 over the Background of the Invention section in view of Kablanian et al. and Sample et al., U.S. Patent No. 5,841,967, (iv) claims 8, 9 and 10 are patentable under 35 U.S.C. §103 over the Background of the Invention section in view of Kablanian et al. and Higgins et al., U.S. Patent No. 6,397,349, (v) claim 11 is patentable under 35 U.S.C. §103 over the Background of the Invention section in view of Kablanian et al., Higgins et al. and Official Notice that it is well known in the art to store coordinates in memory for future use or to create a permanent record and (vi) claim 20 is patentable under 35 U.S.C. §103 over the Background of the Invention section in view of Kablanian et al. and Official Notice that it is well known in the art to write files for future user or to create a permanent record.

VII. GROUPING OF CLAIMS

Appellants contend that the claims of the present invention do not stand or fall together. In particular, the following groups of claims are separately patentable:

Group 1: Claims 1, 14, 15 and 16 stand together.

Group 2: Claims 12 and 20 stand together.

Group 3: Claim 13 stands alone.

Group 4: Claims 2 and 3 stand together.

Group 5: Claim 4 stands alone.

Group 6: Claims 5 and 6 stand together.

Group 7: Claim 7 stands alone.

Group 8: Claims 8, 10 and 11 stand together.

Group 9: Claims 9 and 17 stand together.

Group 10: Claims 18 and 19 stand together.

The claim(s) in each group is (are) separately patentable from the claim(s) in any other groups.

VIII. ARGUMENTS

A. Selected groupings of claims are each patentable under 35 U.S.C. §112.

35 U.S.C. § 112

1. **Group 1 (claims 1, 14, 15, and 16) is patentable under 35 U.S.C. §112, first paragraph.**

The Examiner must provide a reasonable basis to question the enablement provide for the claimed invention.¹ The Examiner has not established a *prima facie* case that pending claim 1 is not disclosed in the specification as originally filed in compliance with the enablement portion of 35 U.S.C. §112, first paragraph. Furthermore, the specification as originally filed does meet the enablement description requirements of 35 U.S.C. §112, first paragraph. As such, the claimed invention is fully compliant with 35 U.S.C. §112, first paragraph and the rejection should be reversed.

Regarding the enablement rejection for claim 1, the Examiner has stated that “The specification does not adequately describe this phrase.”² The Examiner’s arguments are merely conclusory statements. The Examiner has not meet the initial burden to provided a reasonable basis to question the enablement. Therefore, a *prima facie* case for non-enablement has not been established.

Furthermore, the claim 1 step “simulating said design with at least one of said fuses programmed for said repair to verify said repair” is described in the specification as follows:

¹ Manual of Patent Examining Procedures (M.P.E.P.), Eighth Edition, Revised February 2003, §2164.04.

² Office Action, January 10, 2003, page 7, item 32.

The repair block 120 may be exercised in advance of the first-silicon for specific part failures. The repair block 120 may predict fuse locations that, if programmed, may correct a part experiencing failure. The method 100 may provide an easy and reliable method to perform simulations that emulate a design as if those locations were programmed on the die by the laser.³

One of ordinary skill in the art would understand simulating a design with a programmed fuse in advance of the first silicon of the design. As such, claim 1 is enabled and the Examiner has failed to establish a *prima facie* case for non-enablement, thus the rejection should be reversed.

2. Group 7 (claim7) is patentable under 35 U.S.C. §112, first paragraph and second paragraph.

The Examiner must provide a reasonable basis to question the enablement provide for the claimed invention.⁴ The Examiner has not established a *prima facie* case that pending claim 7 is not disclosed in the specification as originally filed in compliance with the enablement portion of 35 U.S.C. §112, first paragraph. The specification as originally filed does meet the enablement description requirements of 35 U.S.C. §112, first paragraph. The Examiner has not provide any evidence that claim 7 is indefinite. Furthermore, the claim does particularly point out and distinctly define the metes and bounds of the subject matter regarded as the invention. As such, the claimed invention is fully compliant with 35 U.S.C. §112, first paragraph and second paragraph and the rejections should be reversed.

³ Application, page 9, lines 13-19 as originally filed.

⁴ M.P.E.P., Eighth Edition, Revised February 2003, §2164.04.
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Regarding the enablement rejection for claim 7, the Examiner has stated that “The specification does not adequately describe this phrase.”⁵ The Examiner’s argument is merely a conclusory statement. The Examiner has not meet the initial burden to provided a reasonable basis to question the enablement. Therefore, a *prima facie* case for non-enablement has not been established.

Furthermore, the claim 7 step “generating a repair file that predicts said at least one of said fuses programmed for said repair” is described in the specification as follows:

Construction of the repair block 120 may rely on part-specific redundancy information and errors found after a first-silicon delay part production. The repair block 120 may receive the errors from the defect block 122.⁶

One of ordinary skill in the art would understand how to construct a program file using detected errors supplied by another block.

Regarding the indefiniteness rejection, claim 7 does set forth the subject matter that the Appellants regards as the invention and particularly points out and distinctly defines the metes and bounds of the subject matter.⁷ The subject matter regarded as the invention is a subjective test that is satisfied as evidenced by the submission of claim 7 for examination. The claim 7 step “generating a repair file that predicts the at least one of the fuses programmed for repair” meets the objective test to define the metes and bounds of the subject matter by adding a limitation to generate a repair file along with an explanation of what the repair file is for. Therefore, claim 7 is definite under 35 U.S.C. §112, second paragraph.

⁵ Office Action, January 10, 2003, page 7, item 33.

⁶Application, page 9, lines 10-13 as originally filed.

⁷ M.P.E.P. Eighth Edition, Revised February 2003, §2171.

Furthermore, the Examiner's argument for rejecting claim 7 is, "This phrase is not adequately defined."⁸ The Examiner is merely making a conclusory statement that does not explain why the claim language (i) fails to set forth the subject matter regarded as the invention or (ii) fails to particularly point out and distinctly define the metes and bounds of the subject matter. Therefore, the Examiner has failed to establish a sufficiently clear basis for the rejection of claim 7 to permit the Appellants an opportunity to correct the alleged problem. As such, claim 7 is enabled, definite, the Examiner has failed to establish a *prima facie* case for non-enablement and the Examiner has failed to provide any evidence of indefiniteness, thus the rejections should be reversed.

B. Selected groupings of the claims are each patentable over the Background of the Invention section of the application in view of Kablanian et al., Tzori, Sample et al., Higgins et al. and Official Notice taken by the Examiner.

35 U.S.C. § 103

"[T]o establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the applicants."⁹ "[T]he factual inquiry whether to combine references must be thorough and searching."¹⁰ "This factual question ... [cannot] be resolved on

⁸ Office Action, January 10, 2003, page 8, item 39.

⁹ *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1316 (Fed. Cir. 2000) (citing *In re Dance*, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); *In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984)).

¹⁰ *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1351-52, 60 USPQ2d 1001, 1008 (Fed. Cir. 2001).

subjective belief and unknown authority.”¹¹ “It must be based on objective evidence of record.”¹² The Examiner must show that (a) there is some suggestion or motivation, either in the references or in the knowledge generally available to one of ordinary skill in the art, to modify or combine the references, (b) there is a reasonable expectation of success, and (c) the prior art reference (or combination of references) teaches or suggests all of the claim limitations.¹³ Furthermore, The Court of Appeals for the Federal Circuit has indicated that the requirement for showing the teaching of motivation to combine references is “rigorous” and must be “clear and particular”.¹⁴

1. Group 1 (claims 1, 14, 15, and 16) is patentable over the Background of the Invention section in view of Kablanian et al.

The Examiner has failed to establish a *prima facie* case for obviousness to combine the Background of the Invention section of the instant application and Kablanian et al. No admission has been made and no evidence has been provided that the Background of the Invention section is prior art. The Examiner has not provided clear and particular evidence of motivation to combine the Background of the Invention section with Kablanian et al. Furthermore, conflicting interpretations regarding two sentences from the Background of the Invention section exist in the final Office Action. Even if the proposed combination was made, the proposed combination still does not teach or suggest simulating a design with at least one of a plurality of fuses programmed for a repair to

¹¹ *In re Lee*, 277 F.3d 1338, 1343-44, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002).

¹² *Id.* at 1343, 61 USPQ2d at 1434.

¹³ M.P.E.P., Eighth Edition, Revised February 2003. §2142.

¹⁴ *In re Anita Dembiczak and Benson Zinbarg*, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999)

verify the repair. As such, the claimed invention is fully patentable over the cited references and the rejection should be reversed.

The Examiner has failed to establish a *prima facie* case of obviousness for lack of evidence that the prior art references teach or suggest all of the claim limitations. In particular, the Background of the Invention section of any application may include:

A paragraph(s) describing to the extent practical the state of the prior art **or other information disclosed known to the applicant**, including references to specific prior art or other information where appropriate.¹⁵ (Emphasis added by Appellants' representative)

No admission has been made that any statements in the Background of the Invention section of the instant application is prior art. No evidence has been provided by the Examiner that any statement in the Background of the Invention section of the instant application qualifies as prior art. No evidence has been provided by the Examiner that any admission has been made by the Appellants. Therefore, the Examiner has failed to establish that the sentences relied upon for the 35 U.S.C. §103(a) rejection are prior art. Writing sentences in the Background of the Invention section of an application does not automatically imply that the sentences are admissions of prior art. As such, the Examiner has failed to establish a *prima facie* case of obviousness for lack of evidence that the prior art references teach or suggest all of the claim limitations.

The Examiner has failed to establish a *prima facie* case of obviousness for lack of clear and particular motivation to combine the Background of the Invention section of the instant application with Kablanian et al. In particular, (i) no evidence of a reasonable expectation of success has been provided and (ii) the asserted motivation is a conclusory statement. As such, the claimed invention is fully patentable over the proposed combination and the rejections should be reversed.

¹⁵ M.P.E.P., Eighth Edition, Revised February 2003, §608.01(c).
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The proposed combination appears to add external software for optimizing redundant memory lines and fuse/anti-fuse equipment taught by Kablanian et al. to manual procedures and conventional methods disclosed in the Background of the Invention section. The Examiner has not provided any evidence regarding a reasonable expectation for success of the proposed combination. Therefore, a *prima facie* case for obviousness has not been established for lack of clear and particular evidence of a reasonable expectation of success.

Furthermore, the asserted motivation to “determine the optimal utilization”¹⁶ is a conclusory statement taken out of context. The Background of the Invention section discusses enumeration of fuse locations and verification of a repair using the fuses. In contrast, the full context provided by Kablanian et al. for “optimal utilization” applies to redundant memory lines used to repair defective memory lines. The Background of the Invention section makes no references to memory lines or optimization. Therefore, there is no clear and particular motivation why one of ordinary skill in the art working on fuse enumeration and repair verification would seek a memory line optimization reference such as Kablanian et al. The fact that references can be combined is not sufficient to establish obviousness.¹⁷ Therefore, the Examiner has failed to establish a *prima facie* case of obviousness for lack of (i) evidence for a reasonable expectation of success and (ii) evidence of motivation to combine or modify the references.

Claim 1 provides simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair. Assuming, *arguendo*, that the proposed combination of the Background of the Invention and Kablanian et al. would have been obvious (for which the

¹⁶ Office Action, January 10, 2003, page 9, item 56.

¹⁷ M.P.E.P., Eighth Edition, Revised February 2003, §2143.01.

Appellants' representative does not necessarily agree), the proposed combination still does not teach every element of the pending claims. Despite the Examiner's suggestion¹⁸, Kablanian et al. do not teach or suggest simulating a design with at least one fuse programmed for a repair to verify the repair. **Determining** an optimum utilization of redundant memory lines to repair defective memory lines takes place **before** the repair is performed. In contrast, the claim provides **verifying** the repair **after** simulating the repair.

Furthermore, the Examiner has interpreted the "external software" taught by Kablanian et al. to include simulation software that simulates the repair.¹⁹ However, the Examiner appears to have used the claim language as a template to change the plain meaning of Kablanian et al. Nothing in Kablanian et al. teaches or suggests that the external software performs a simulation of the memory circuit or performs a simulation of a repair to the memory circuit. In contrast, Kablanian et al. teach repairing an actual chip using a conventional laser beam and then retesting the actual chip with automatic test equipment (ATE).²⁰ Using a conventional laser and ATE does not teach or suggest simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair as presently claimed. Therefore, the proposed combination does not teach or suggest every element as presently claimed and the rejections should be reversed.

The Examiner has failed to establish a *prima facie* case for obviousness because the proposed combination of the Background of the Invention section and Kablanian et al. does not provide clear and particular evidence of a teaching or suggestion for the claimed data for each of a

¹⁸ Office Action, January 10, 2003, page 9, item 55.

¹⁹ Advisory Action, March 24, 2003, page 2, item 13.

²⁰ Kablanian et al., column 2, lines 7-14.

plurality of fuses. In particular, the rationale for the claim 1 rejection makes conflicting statements within the final Office Action regarding two sentences in the Background of the Invention section which read:

The conventional methods to manually associate the fuse path to the fuse locations, or vice versa, use a layout versus schematic (LVS) cross-probe user-interface. Conventional verilog simulation paths are derived by manual translation of schematic paths aided by visual inspection of a netlist.²¹

Claim 1 provides compiling data for each of a plurality of fuses, wherein the data comprises simulation path data. The Examiner has asserted that the two sentences in the Background of the Invention section teach compiling data for each one of a plurality of fuses, wherein the data comprises **simulation path data**.²² In addition, the Examiner has also asserted that the same two sentences teach that the data comprises **schematic path data**.²³ Furthermore, the Examiner has asserted that the same two sentences teach that the data comprises **physical layout data**.²⁴ The same two sentences cannot teach or suggest three different types of data simultaneously. Therefore, no clear and particular evidence has been provided that the Background of the Invention section teaches or suggests compiling data for each of a plurality of fuses, wherein the data comprises simulation path data as presently claimed. As such, the Examiner has failed to establish a *prima facie* case for obviousness due to conflicting interpretations of the Background of the Invention section.

In summary, a *prima facie* case for obviousness has not been established to combine the Background of the Invention section of the instant application and Kablanian et al. No admission

²¹ Application, page 1, lines 16-20 as originally filed.

²² Office Action, January 10, 2003, page 9, item 52.

²³ Office Action, January 10, 2003, page 15, item 103.

²⁴ Office Action, January 10, 2003, page 15, item 106.

has been made that the Background of the Invention section is prior art. No evidence has been provided by the Examiner that the cited sentences in the Background of the Invention section qualify as prior art. The Examiner has not provided clear and particular evidence of motivation to combine the Background of the Invention section with Kablanian et al. Furthermore, the Examiner has made conflicting interpretations regarding two sentences from the Background of the Invention section relied upon in the rejections. Even if the Background of the Invention section was prior art and the proposed combination were made, the proposed combination still does not teach or suggest simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair as presently claimed. As such, the claimed invention is fully patentable over the cited references and the rejections should be reversed.

2. Group 2 (claims 12 and 20) is patentable over the Background of the Invention section in view of Kablanian et al.

The Examiner has failed to establish a *prima facie* case for obviousness to combine the Background of the Invention section of the instant application and Kablanian et al. No admission has been made and no evidence has been provided that the Background of the Invention section is prior art. The Examiner has not provided clear and particular evidence of motivation to combine the Background of the Invention section with Kablanian et al. Furthermore, conflicting interpretations regarding two sentences from the Background of the Invention section exist in the final Office Action. Even if the proposed combination was made, the proposed combination still does not teach or suggest (i) a first circuit, (ii) a second circuit and (iii) simulating a design with at least one of a

plurality of fuses programmed for a repair to verify the repair. As such, the claimed invention is fully patentable over the cited references and the rejections should be reversed.

The Examiner has failed to establish a *prima facie* case of obviousness for lack of evidence that the prior art references teach or suggest all of the claim limitations. In particular, the Background of the Invention section of any application may include:

A paragraph(s) describing to the extent practical the state of the prior art **or other information disclosed known to the applicant**, including references to specific prior art or other information where appropriate.²⁵ (Emphasis added by Appellants' representative)

No admission has been made that any statements in the Background of the Invention section of the instant application is prior art. No evidence has been provided by the Examiner that any statement in the Background of the Invention section of the instant application qualifies as prior art. No evidence has been provided by the Examiner that any admission has been made by the Appellants. Therefore, the Examiner has failed to establish that the sentences relied upon for the 35 U.S.C. §103(a) rejection are prior art. Writing sentences in the Background of the Invention section of an application does not automatically imply that the sentences are admissions of prior art. As such, the Examiner has failed to establish a *prima facie* case of obviousness for lack of evidence that the prior art references teach or suggest all of the claim limitations.

The Examiner has failed to establish a *prima facie* case of obviousness for lack of clear and particular motivation to combine the Background of the Invention section of the instant application with Kablanian et al. In particular, (i) no evidence of a reasonable expectation of success has been provided and (ii) the asserted motivation is a conclusory statement. As such, the claimed invention is fully patentable over the proposed combination and the rejections should be reversed.

²⁵ M.P.E.P., Eighth Edition, Revised February 2003, §608.01(c).
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The proposed combination appears to add external software for optimizing redundant memory lines and fuse/anti-fuse equipment taught by Kablanian et al. to manual procedures and conventional methods disclosed in the Background of the Invention section. The Examiner has not provided any evidence regarding a reasonable expectation for success of the proposed combination. Therefore, a *prima facie* case for obviousness has not been established for lack of clear and particular evidence of a reasonable expectation of success.

Furthermore, the asserted motivation to “determine the optimal utilization”²⁶ is a conclusory statement taken out of context. The Background of the Invention section discusses enumeration of fuse locations and verification of a repair using the fuses. In contrast, the full context provided by Kablanian et al. for “optimal utilization” applies to redundant memory lines used to repair defective memory lines. The Background of the Invention section makes no references to memory lines or optimization. Therefore, there is no clear and particular motivation why one of ordinary skill in the art working on fuse enumeration and repair verification would seek a memory line optimization reference such as Kablanian et al. The fact that references can be combined is not sufficient to establish obviousness.²⁷ Therefore, the Examiner has failed to establish a *prima facie* case of obviousness for lack of (i) evidence for a reasonable expectation of success and (ii) evidence of motivation to combine or modify the references.

Claim 12 provides a second circuit configured to perform a simulation of the design with at least one of a plurality of fuses programmed for a repair of the design to verify a repair. Assuming, *arguendo*, that the proposed combination of the Background of the Invention and

²⁶ Office Action, January 10, 2003, page 9, item 56.

²⁷ M.P.E.P., Eighth Edition, Revised February 2003, §2143.01.
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Kablanian et al. would have been obvious (for which the Appellants' representative does not necessarily agree), the proposed combination still does not teach every element of the pending claims. Despite the Examiner's suggestion²⁸, Kablanian et al. do not teach or suggest simulating a design with at least one fuse programmed for a repair to verify the repair. **Determining** an optimum utilization of redundant memory lines to repair defective memory lines takes place **before** the repair is performed. In contrast, the claim provides **verifying** the repair **after** simulating the repair.

Furthermore, the Examiner has interpreted the "external software" taught by Kablanian et al. to include simulation software that simulates the repair.²⁹ However, the Examiner appears to have used the claim language as a template to change the plain meaning of Kablanian et al. Nothing in Kablanian et al. teaches or suggests that the external software performs a simulation of the memory circuit or performs a simulation of a repair to the memory circuit. External software is also not a circuit as per claim 12. In contrast, Kablanian et al. teach repairing an actual chip using a conventional laser beam and then retesting the actual chip with automatic test equipment (ATE).³⁰ Using a conventional laser and ATE does not teach or suggest simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair as presently claimed. Therefore, the proposed combination does not teach or suggest every element as presently claimed and the rejections should be reversed.

The Examiner has failed to establish a *prima facie* case for obviousness because the proposed combination of the Background of the Invention section and Kablanian et al. does not

²⁸ Office Action, January 10, 2003, page 9, item 55.

²⁹ Advisory Action, March 24, 2003, page 2, item 13.

³⁰ Kablanian et al., column 2, lines 7-14.

provide clear and particular evidence of a teaching or suggestion for the claimed data for each of a plurality of fuses. In particular, the rationale for the claim 12 rejection makes conflicting statements within the final Office Action regarding two sentences in the Background of the Invention section which read:

The conventional methods to manually associate the fuse path to the fuse locations, or vice versa, use a layout versus schematic (LVS) cross-probe user-interface. Conventional verilog simulation paths are derived by manual translation of schematic paths aided by visual inspection of a netlist.³¹

Claim 12 provides compiling data for each of a plurality of fuses, wherein the data comprises simulation path data. The Examiner has asserted that the two sentences in the Background of the Invention section teach compiling data for each one of a plurality of fuses, wherein the data comprises **simulation path data**.³² In addition, the Examiner has also asserted that the same two sentences teach that the data comprises **schematic path data**.³³ Furthermore, the Examiner has asserted that the same two sentences teach that the data comprises **physical layout data**.³⁴ The same two sentences cannot teach or suggest three different types of data simultaneously. Therefore, no clear and particular evidence has been provided that the Background of the Invention section teaches or suggests compiling data for each of a plurality of fuses, wherein the data comprises simulation path data as presently claimed. As such, the Examiner has failed to establish a *prima facie* case for obviousness due to conflicting interpretations of the Background of the Invention section.

³¹ Application, page 1, lines 16-20 as originally filed.

³² Office Action, January 10, 2003, page 9, item 52.

³³ Office Action, January 10, 2003, page 15, item 103.

³⁴ Office Action, January 10, 2003, page 15, item 106.

The Examiner has failed to establish a *prima facie* case for obviousness for lack of evidence for every element of the claim. Claim 12 provides a first circuit and a second circuit. No evidence has been provided by the Examiner that the references teach or suggest a first circuit or a second circuit as presently claimed.³⁵ Therefore, the Examiner has failed to establish that the Background of the Invention section and Kablanian et al. alone, or in combination, teach or suggest every element as presently claimed.

In summary, a *prima facie* case for obviousness has not been established to combine the Background of the Invention section of the instant application and Kablanian et al. No admission has been made that the Background of the Invention section is prior art. No evidence has been provided by the Examiner that the cited sentences in the Background of the Invention section qualify as prior art. The Examiner has not provided clear and particular evidence of motivation to combine the Background of the Invention section with Kablanian et al. Furthermore, the Examiner has made conflicting interpretations regarding two sentences from the Background of the Invention section relied upon in the rejections. Even if the Background of the Invention section was prior art and the proposed combination were made, the proposed combination still does not teach or suggest (i) a first circuit, (ii) a second circuit and (iii) simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair as presently claimed. As such, the claimed invention is fully patentable over the cited references and the rejections should be reversed.

³⁵ Office Action, January 10, 2003, page 14, item 98.
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3. **Group 3 (claim 13) is patentable over the Background of the Invention section in view of Kablanian et al.**

The Examiner has failed to establish a *prima facie* case for obviousness to combine the Background of the Invention section of the instant application and Kablanian et al. No admission has been made and no evidence has been provided that the Background of the Invention section is prior art. The Examiner has not provided clear and particular evidence of motivation to combine the Background of the Invention section with Kablanian et al. Furthermore, conflicting interpretations regarding two sentences from the Background of the Invention section exist in the final Office Action. Even if the proposed combination was made, the proposed combination still does not teach or suggest (i) a means for generating, (ii) a means for compiling, (iii) a means for simulating and (iv) simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair. As such, the claimed invention is fully patentable over the cited references and the rejection should be reversed.

The Examiner has failed to establish a *prima facie* case of obviousness for lack of evidence that the prior art references teach or suggest all of the claim limitations. In particular, the Background of the Invention section of any application may include:

A paragraph(s) describing to the extent practical the state of the prior art **or other information disclosed known to the applicant**, including references to specific prior art or other information where appropriate.³⁶ (Emphasis added by Appellants' representative)

No admission has been made that any statements in the Background of the Invention section of the instant application is prior art. No evidence has been provided by the Examiner that any statement in the Background of the Invention section of the instant application qualifies as prior art. No

³⁶ M.P.E.P., Eighth Edition, Revised February 2003, §608.01(c).
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evidence has been provided by the Examiner that any admission has been made by the Appellants. Therefore, the Examiner has failed to establish that the sentences relied upon for the 35 U.S.C. §103(a) rejection are prior art. Writing sentences in the Background of the Invention section of an application does not automatically imply that the sentences are admissions of prior art. As such, the Examiner has failed to establish a *prima facie* case of obviousness for lack of evidence that the prior art references teach or suggest all of the claim limitations.

The Examiner has failed to establish a *prima facie* case of obviousness for lack of clear and particular motivation to combine the Background of the Invention section of the instant application with Kablanian et al. In particular, (i) no evidence of a reasonable expectation of success has been provided and (ii) the asserted motivation is a conclusory statement. As such, the claimed invention is fully patentable over the proposed combination and the rejection should be reversed.

The proposed combination appears to add external software for optimizing redundant memory lines and fuse/anti-fuse equipment taught by Kablanian et al. to manual procedures and conventional methods disclosed in the Background of the Invention section. The Examiner has not provided any evidence regarding a reasonable expectation for success of the proposed combination. Therefore, a *prima facie* case for obviousness has not been established for lack of clear and particular evidence of a reasonable expectation of success.

Furthermore, the asserted motivation to “determine the optimal utilization”³⁷ is a conclusory statement taken out of context. The Background of the Invention section discusses enumeration of fuse locations and verification of a repair using the fuses. In contrast, the full context provided by Kablanian et al. for “optimal utilization” applies to redundant memory lines used to

³⁷ Office Action, January 10, 2003, page 9, item 56.
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repair defective memory lines. The Background of the Invention section makes no references to memory lines or optimization. Therefore, there is no clear and particular motivation why one of ordinary skill in the art working on fuse enumeration and repair verification would seek a memory line optimization reference such as Kablanian et al. The fact that references can be combined is not sufficient to establish obviousness.³⁸ Therefore, the Examiner has failed to establish a *prima facie* case of obviousness for lack of (i) evidence for a reasonable expectation of success and (ii) evidence of motivation to combine or modify the references.

Claim 13 provides a means for generating, a means for compiling, a means for simulating and a simulating of the design with at least one of a plurality of fuses programmed for a repair of the design to verify the repair. Assuming, *arguendo*, that the proposed combination of the Background of the Invention and Kablanian et al. would have been obvious (for which the Appellants' representative does not necessarily agree), the proposed combination still does not teach every element of the pending claims. Despite the Examiner's suggestion³⁹, Kablanian et al. do not teach or suggest simulating a design with at least one fuse programmed for a repair to verify the repair. **Determining** an optimum utilization of redundant memory lines to repair defective memory lines takes place **before** the repair is performed. In contrast, the claim provides **verifying** the repair **after** simulating the repair.

Furthermore, the Examiner has interpreted the "external software" taught by Kablanian et al. to include simulation software that simulates the repair.⁴⁰ However, the Examiner

³⁸ M.P.E.P., Eighth Edition, Revised February 2003, §2143.01.

³⁹ Office Action, January 10, 2003, page 9, item 55.

⁴⁰ Advisory Action, March 24, 2003, page 2, item 13.

appears to have used the claim language as a template to change the plain meaning of Kablanian et al. Nothing in Kablanian et al. teaches or suggests that the external software performs a simulation of the memory circuit or performs a simulation of a repair to the memory circuit. External software also fails to teach or suggest the structure of a means for generating, a means for compiling and a means for simulating. In contrast, Kablanian et al. teach repairing an actual chip using a conventional laser beam and then retesting the actual chip with automatic test equipment (ATE).⁴¹ Using a conventional laser and ATE does not teach or suggest simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair as presently claimed. Therefore, the proposed combination does not teach or suggest every element as presently claimed and the rejection should be reversed.

The Examiner has failed to establish a *prima facie* case for obviousness because the proposed combination of the Background of the Invention section and Kablanian et al. do not provide clear and particular evidence of a teaching or suggestion for the claimed data for each of a plurality of fuses. In particular, the rationale for the claim 13 rejection makes conflicting statements within the final Office Action regarding two sentences in the Background of the Invention section which read:

The conventional methods to manually associate the fuse path to the fuse locations, or vice versa, use a layout versus schematic (LVS) cross-probe user-interface. Conventional verilog simulation paths are derived by manual translation of schematic paths aided by visual inspection of a netlist.⁴²

Claim 13 provides compiling data for each of a plurality of fuses, wherein the data comprises simulation path data. The Examiner has asserted that the two sentences in the Background of the

⁴¹ Kablanian et al., column 2, lines 7-14.

⁴² Application, page 1, lines 16-20 as originally filed.

Invention section teach compiling data for each one of a plurality of fuses, wherein the data comprises **simulation path data**.⁴³ In addition, the Examiner has also asserted that the same two sentences teach that the data comprises **schematic path data**.⁴⁴ Furthermore, the Examiner has asserted that the same two sentences teach that the data comprises **physical layout data**.⁴⁵ The same two sentences cannot teach or suggest three different types of data simultaneously. Therefore, no clear and particular evidence has been provided that the Background of the Invention section teaches or suggests compiling data for each of a plurality of fuses, wherein the data comprises simulation path data as presently claimed. As such, the Examiner has failed to establish a *prima facie* case for obviousness due to conflicting interpretations of the Background of the Invention section.

The Examiner has failed to establish a *prima facie* case for obviousness for lack of evidence for every element of the claim. Claim 13 provides a structure of a means for generating, a means for compiling and a means for simulating. No evidence was provided by the Examiner that the references teach or suggest a means for generating, a means for compiling and a means for simulating as presently claimed.⁴⁶ Therefore, the Examiner has failed to establish that the Background of the Invention section and Kablanian et al. alone, or in combination, teach or suggest every element as presently claimed.

In summary, a *prima facie* case for obviousness has not been established to combine the Background of the Invention section of the instant application and Kablanian et al. No admission

⁴³ Office Action, January 10, 2003, page 9, item 52.

⁴⁴ Office Action, January 10, 2003, page 15, item 103.

⁴⁵ Office Action, January 10, 2003, page 15, item 106.

⁴⁶ Office Action, January 10, 2003, page 14, item 100.

has been made that the Background of the Invention section is prior art. No evidence has been provided by the Examiner that the cited sentences in the Background of the Invention section qualify as prior art. The Examiner has not provided clear and particular evidence of motivation to combine the Background of the Invention section with Kablanian et al. Furthermore, the Examiner has made conflicting interpretations regarding two sentences from the Background of the Invention section relied upon in the rejection. Even if the Background of the Invention section was prior art and the proposed combination were made, the proposed combination still does not teach or suggest (i) a means for generating, (ii) a means for compiling, (iii) a means for simulating and (iv) simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair as presently claimed. As such, the claimed invention is fully patentable over the cited references and the rejection should be reversed.

4. Group 6 (claims 5 and 6) is patentable over the Background of the Invention section in view of Kablanian et al.

The Examiner has failed to establish a *prima facie* case for obviousness to combine the Background of the Invention section of the instant application and Kablanian et al. No admission has been made and no evidence has been provided that the Background of the Invention section is prior art. The Examiner has not provided clear and particular evidence of motivation to combine the Background of the Invention section with Kablanian et al. Furthermore, multiple conflicting interpretations regarding three sentences from the Background of the Invention section exist in the final Office Action. Even if the proposed combination was made, the proposed combination still does not teach or suggest simulating a design with at least one of a plurality of fuses programmed

for a repair to verify the repair. As such, the claimed invention is fully patentable over the cited references and the rejections should be reversed.

The Examiner has failed to establish a *prima facie* case of obviousness for lack of evidence that the prior art references teach or suggest all of the claim limitations. In particular, the Background of the Invention section of any application may include:

A paragraph(s) describing to the extent practical the state of the prior art **or other information disclosed known to the applicant**, including references to specific prior art or other information where appropriate.⁴⁷ (Emphasis added by Appellants' representative)

No admission has been made that any statements in the Background of the Invention section of the instant application is prior art. No evidence has been provided by the Examiner that any statement in the Background of the Invention section of the instant application qualifies as prior art. No evidence has been provided by the Examiner that any admission has been made by the Appellants. Therefore, the Examiner has failed to establish that the sentences relied upon for the 35 U.S.C. §103(a) rejection are prior art. Writing sentences in the Background of the Invention section of an application does not automatically imply that the sentences are admissions of prior art. As such, the Examiner has failed to establish a *prima facie* case of obviousness for lack of evidence that the prior art references teach or suggest all of the claim limitations.

The Examiner has failed to establish a *prima facie* case of obviousness for lack of clear and particular motivation to combine the Background of the Invention section of the instant application with Kablanian et al. In particular, (i) no evidence of a reasonable expectation of success has been provided and (ii) the asserted motivation is a conclusory statement. As such, the claimed invention is fully patentable over the proposed combination and the rejections should be reversed.

⁴⁷ M.P.E.P., Eighth Edition, Revised February 2003, §608.01(c).
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The proposed combination appears to add external software for optimizing redundant memory lines and fuse/anti-fuse equipment taught by Kablanian et al. to manual procedures and conventional methods disclosed in the Background of the Invention section. The Examiner has not provided any evidence regarding a reasonable expectation for success of the proposed combination. Therefore, a *prima facie* case for obviousness has not been established for lack of clear and particular evidence of a reasonable expectation of success.

Furthermore, the asserted motivation to “determine the optimal utilization”⁴⁸ is a conclusory statement taken out of context. The Background of the Invention section discusses enumeration of fuse locations and verification of a repair using the fuses. In contrast, the full context provided by Kablanian et al. for “optimal utilization” applies to redundant memory lines used to repair defective memory lines. The Background of the Invention section makes no references to memory lines or optimization. Therefore, there is no clear and particular motivation why one of ordinary skill in the art working on fuse enumeration and repair verification would seek a memory line optimization reference such as Kablanian et al. The fact that references can be combined is not sufficient to establish obviousness.⁴⁹ Therefore, the Examiner has failed to establish a *prima facie* case of obviousness for lack of (i) evidence for a reasonable expectation of success and (ii) evidence of motivation to combine or modify the references.

Claims 5 and 6, by dependency from claim 1, provide simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair. Assuming, *arguendo*, that the proposed combination of the Background of the Invention and Kablanian et al. would have

⁴⁸ Office Action, January 10, 2003, page 9, item 56.

⁴⁹ M.P.E.P., Eighth Edition, Revised February 2003, §2143.01.
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been obvious (for which the Appellants' representative does not necessarily agree), the proposed combination still does not teach every element of the pending claims. Despite the Examiner's suggestion⁵⁰, Kablanian et al. do not teach or suggest simulating a design with at least one fuse programmed for a repair to verify the repair. **Determining** an optimum utilization of redundant memory lines to repair defective memory lines takes place **before** the repair is performed. In contrast, the claim provides **verifying** the repair **after** simulating the repair.

Furthermore, the Examiner has interpreted the "external software" taught by Kablanian et al. to include simulation software that simulates the repair.⁵¹ However, the Examiner appears to have used the claim language as a template to change the plain meaning of Kablanian et al. Nothing in Kablanian et al. teaches or suggests that the external software performs a simulation of the memory circuit or performs a simulation of a repair to the memory circuit. In contrast, Kablanian et al. teach repairing an actual chip using a conventional laser beam and then retesting the actual chip with automatic test equipment (ATE).⁵² Using a conventional laser and ATE does not teach or suggest simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair as presently claimed. Therefore, the proposed combination does not teach or suggest every element as presently claimed and the rejections should be reversed.

The Examiner has failed to establish a *prima facie* case for obviousness because the proposed combination of the Background of the Invention section and Kablanian et al. do not provide clear and particular evidence of a teaching or suggestion for the claimed data for each of a

⁵⁰ Office Action, January 10, 2003, page 9, item 55.

⁵¹ Advisory Action, March 24, 2003, page 2, item 13.

⁵² Kablanian et al., column 2, lines 7-14.

plurality of fuses. In particular, the rational for the claim rejections make conflicting statements within the final Office Action regarding two sentences in the Background of the Invention section which read:

The conventional methods to manually associate the fuse path to the fuse locations, or vise versa, use a layout versus schematic (LVS) cross-probe user-interface. Conventional verilog simulation paths are derived by manual translation of schematic paths aided by visual inspection of a netlist.⁵³

Claims 5 and 6, through dependency from claim 1, provide compiling data for each of a plurality of fuses, wherein the data comprises simulation path data. The Examiner has asserted that the two sentences in the Background of the Invention section teach compiling data for each one of a plurality of fuses, wherein the data comprises **simulation path data**.⁵⁴ In addition, the Examiner has also asserted that the same two sentences teach that the data comprises **schematic path data**.⁵⁵ Furthermore, the Examiner has asserted that the same two sentences teach that the data comprises **physical layout data**.⁵⁶ The same two sentences cannot teach or suggest three different types of data simultaneously. Therefore, no clear and particular evidence has been provided that the Background of the Invention section teaches or suggests compiling data for each of a plurality of fuses, wherein the data comprises simulation path data as presently claimed. As such, the Examiner has failed to establish a *prima facie* case for obviousness due to conflicting interpretations of the Background of the Invention section.

⁵³ Application, page 1, lines 16-20 as originally filed.

⁵⁴ Office Action, January 10, 2003, page 9, item 52.

⁵⁵ Office Action, January 10, 2003, page 15, item 103.

⁵⁶ Office Action, January 10, 2003, page 15, item 106.

Furthermore, the Examiner has made conflicting statements regarding another sentence in the Background of the Invention section of the instant application which reads:

Conventional methods exist to manually associate a fuse path to a fuse location or the fuse location to the fuse path, one at a time.⁵⁷

The Examiner has asserts that the above sentence teaches **generating a fuse report**.⁵⁸ Examiner has further asserted that the same sentence teaches **listing physical locations** of a device in the design in response to the fuse report.⁵⁹ The Examiner has asserted that the same sentence teaches **generating a repair file** that predicts at least one of a plurality of fuses programmed for a repair.⁶⁰ Finally, the Examiner has asserted that the same sentence teaches **listing an output of a repair program** as a list of coordinates for at least one of a plurality fuses programmed for a repair in terms of a plurality of logical addresses.⁶¹ Since the single sentence cannot teach four very different steps, the Examiner has failed to establish clear and particular evidence that the Background of the Invention section and Kablanian et al. alone, or in combination, teach or suggest every claim element.

In summary, a *prima facie* case for obviousness has not been established to combine the Background of the Invention section of the instant application and Kablanian et al. No admission has been made that the Background of the Invention section is prior art. No evidence has been provided by the Examiner that the cited sentences in the Background of the Invention section qualify

⁵⁷ Application, page 1, lines 14-15 as originally filed.

⁵⁸ Office Action, January 10, 2003, page 11, item 74.

⁵⁹ Office Action, January 10, 2003, page 12, item 77.

⁶⁰ Office Action, January 10, 2003, page 12, item 80.

⁶¹ Office Action, January 10, 2003, page 13, item 91.

as prior art. The Examiner has not provided clear and particular evidence of motivation to combine the Background of the Invention section with Kablanian et al. Furthermore, the Examiner has made multiple conflicting interpretations regarding three sentences from the Background of the Invention section relied upon in the rejections. Even if the Background of the Invention section was prior art and the proposed combination were made, the proposed combination still does not teach or suggest simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair as presently claimed. As such, the claimed invention is fully patentable over the cited references and the rejections should be reversed.

5. Group 7 (claim 7) is patentable over the Background of the Invention section in view of Kablanian et al.

The Examiner has failed to establish a *prima facie* case for obviousness to combine the Background of the Invention section of the instant application and Kablanian et al. No admission has been made and no evidence has been provided that the Background of the Invention section is prior art. The Examiner has not provided clear and particular evidence of motivation to combine the Background of the Invention section with Kablanian et al. Furthermore, multiple conflicting interpretations regarding three sentences from the Background of the Invention section exist in the final Office Action. Even if the proposed combination was made, the proposed combination still does not teach or suggest simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair. As such, the claimed invention is fully patentable over the cited references and the rejection should be reversed.

The Examiner has failed to establish a *prima facie* case of obviousness for lack of evidence that the prior art references teach or suggest all of the claim limitations. In particular, the Background of the Invention section of any application may include:

A paragraph(s) describing to the extent practical the state of the prior art **or other information disclosed known to the applicant**, including references to specific prior art or other information where appropriate.⁶² (Emphasis added by Appellants' representative)

No admission has been made that any statements in the Background of the Invention section of the instant application is prior art. No evidence has been provided by the Examiner that any statement in the Background of the Invention section of the instant application qualifies as prior art. No evidence has been provided by the Examiner that any admission has been made by the Appellants. Therefore, the Examiner has failed to establish that the sentences relied upon for the 35 U.S.C. §103(a) rejection are prior art. Writing sentences in the Background of the Invention section of an application does not automatically imply that the sentences are admissions of prior art. As such, the Examiner has failed to establish a *prima facie* case of obviousness for lack of evidence that the prior art references teach or suggest all of the claim limitations.

The Examiner has failed to establish a *prima facie* case of obviousness for lack of clear and particular motivation to combine the Background of the Invention section of the instant application with Kablanian et al. In particular, (i) no evidence of a reasonable expectation of success has been provided and (ii) the asserted motivation is a conclusory statement. As such, the claimed invention is fully patentable over the proposed combination and the rejection should be reversed.

The proposed combination appears to add external software for optimizing redundant memory lines and fuse/anti-fuse equipment taught by Kablanian et al. to manual procedures and

⁶² M.P.E.P., Eighth Edition, Revised February 2003, §608.01(c).
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conventional methods disclosed in the Background of the Invention section. The Examiner has not provided any evidence regarding a reasonable expectation for success of the proposed combination. Therefore, a *prima facie* case for obviousness has not been established for lack of clear and particular evidence of a reasonable expectation of success.

Furthermore, the asserted motivation to “determine the optimal utilization”⁶³ is a conclusory statement taken out of context. The Background of the Invention section discusses enumeration of fuse locations and verification of a repair using the fuses. In contrast, the full context provided by Kablanian et al. for “optimal utilization” applies to redundant memory lines used to repair defective memory lines. The Background of the Invention section makes no references to memory lines or optimization. Therefore, there is no clear and particular motivation why one of ordinary skill in the art working on fuse enumeration and repair verification would seek a memory line optimization reference such as Kablanian et al. The fact that references can be combined is not sufficient to establish obviousness.⁶⁴ Therefore, the Examiner has failed to establish a *prima facie* case of obviousness for lack of (i) evidence for a reasonable expectation of success and (ii) evidence of motivation to combine or modify the references.

Claim 7, by dependency from claim 1, provides simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair. Assuming, *arguendo*, that the proposed combination of the Background of the Invention and Kablanian et al. would have been obvious (for which the Appellants’ representative does not necessarily agree), the proposed combination still does not teach every element of the pending claims. Despite the Examiner’s

⁶³ Office Action, January 10, 2003, page 9, item 56.

⁶⁴ M.P.E.P., Eighth Edition, Revised February 2003, §2143.01.
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suggestion⁶⁵, Kablanian et al. do not teach or suggest simulating a design with at least one fuse programmed for a repair to verify the repair. **Determining** an optimum utilization of redundant memory lines to repair defective memory lines takes place **before** the repair is performed. In contrast, the claim provides **verifying** the repair **after** simulating the repair.

Furthermore, the Examiner has interpreted the “external software” taught by Kablanian et al. to include simulation software that simulates the repair.⁶⁶ However, the Examiner appears to have used the claim language as a template to change the plain meaning of Kablanian et al. Nothing in Kablanian et al. teaches or suggests that the external software performs a simulation of the memory circuit or performs a simulation of a repair to the memory circuit. In contrast, Kablanian et al. teach repairing an actual chip using a conventional laser beam and then retesting the actual chip with automatic test equipment (ATE).⁶⁷ Using a conventional laser and ATE does not teach or suggest simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair as presently claimed. Therefore, the proposed combination does not teach or suggest every element as presently claimed and the rejection should be reversed.

The Examiner has failed to establish a *prima facie* case for obviousness because the proposed combination of the Background of the Invention section and Kablanian et al. do not provide clear and particular evidence of a teaching or suggestion for the claimed data for each of a plurality of fuses. In particular, the rationale for the claim rejection makes conflicting statements

⁶⁵ Office Action, January 10, 2003, page 9, item 55.

⁶⁶ Advisory Action, March 24, 2003, page 2, item 13.

⁶⁷ Kablanian et al., column 2, lines 7-14.

within the final Office Action regarding two sentences in the Background of the Invention section which read:

The conventional methods to manually associate the fuse path to the fuse locations, or vise versa, use a layout versus schematic (LVS) cross-probe user-interface. Conventional verilog simulation paths are derived by manual translation of schematic paths aided by visual inspection of a netlist.⁶⁸

Claim 7, through dependency from claim 1, provides compiling data for each of a plurality of fuses, wherein the data comprises simulation path data. The Examiner has asserted that the two sentences in the Background of the Invention section teach compiling data for each one of a plurality of fuses, wherein the data comprises **simulation path data**.⁶⁹ In addition, the Examiner has also asserted that the same two sentences teach that the data comprises **schematic path data**.⁷⁰ Furthermore, the Examiner has asserted that the same two sentences teach that the data comprises **physical layout data**.⁷¹ The same two sentences cannot teach or suggest three different types of data simultaneously. Therefore, no clear and particular evidence has been provided that the Background of the Invention section teaches or suggests compiling data for each of a plurality of fuses, wherein the data comprises simulation path data as presently claimed. As such, the Examiner has failed to establish a *prima facie* case for obviousness due to conflicting interpretations of the Background of the Invention section.

Furthermore, the Examiner has made conflicting statements regarding another sentence in the Background of the Invention section of the instant application which reads:

⁶⁸ Application, page 1, lines 16-20 as originally filed.

⁶⁹ Office Action, January 10, 2003, page 9, item 52.

⁷⁰ Office Action, January 10, 2003, page 15, item 103.

⁷¹ Office Action, January 10, 2003, page 15, item 106.

Conventional methods exist to manually associate a fuse path to a fuse location or the fuse location to the fuse path, one at a time.⁷²

The Examiner has asserts that the above sentence teaches **generating a fuse report**.⁷³ Examiner has further asserted that the same sentence teaches **listing physical locations** of a device in the design in response to the fuse report.⁷⁴ The Examiner has asserted that the same sentence teaches **generating a repair file** that predicts at least one of a plurality of fuses programmed for a repair.⁷⁵ Finally, the Examiner has asserted that the same sentence teaches **listing an output of a repair program** as a list of coordinates for at least one of a plurality fuses programmed for a repair in terms of a plurality of logical addresses.⁷⁶ Since the single sentence cannot teach four very different steps, the Examiner has failed to establish clear and particular evidence that the Background of the Invention section and Kablanian et al. alone, or in combination, teach or suggest every claim element.

In summary, a *prima facie* case for obviousness has not been established to combine the Background of the Invention section of the instant application and Kablanian et al. No admission has been made that the Background of the Invention section is prior art. No evidence has been provided by the Examiner that the cited sentences in the Background of the Invention section qualify as prior art. The Examiner has not provided clear and particular evidence of motivation to combine the Background of the Invention section with Kablanian et al. Furthermore, the Examiner has made

⁷² Application, page 1, lines 14-15 as originally filed.

⁷³ Office Action, January 10, 2003, page 11, item 74.

⁷⁴ Office Action, January 10, 2003, page 12, item 77.

⁷⁵ Office Action, January 10, 2003, page 12, item 80.

⁷⁶ Office Action, January 10, 2003, page 13, item 91.

multiple conflicting interpretations regarding three sentences from the Background of the Invention section relied upon in the rejection. Even if the Background of the Invention section was prior art and the proposed combination were made, the proposed combination still does not teach or suggest simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair as presently claimed. As such, the claimed invention is fully patentable over the cited references and the rejection should be reversed.

6. Group 10 (claims 18 and 19) is patentable over the Background of the Invention section in view of Kablanian et al.

The Examiner has failed to establish a *prima facie* case for obviousness to combine the Background of the Invention section of the instant application and Kablanian et al. No admission has been made and no evidence has been provided that the Background of the Invention section is prior art. The Examiner has not provided clear and particular evidence of motivation to combine the Background of the Invention section with Kablanian et al. Furthermore, multiple conflicting interpretations regarding two sentences from the Background of the Invention section exist in the final Office Action. Even if the proposed combination was made, the proposed combination still does not teach or suggest (i) a first circuit, (ii) a second circuit and (iii) simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair. As such, the claimed invention is fully patentable over the cited references and the rejections should be reversed.

The Examiner has failed to establish a *prima facie* case of obviousness for lack of evidence that the prior art references teach or suggest all of the claim limitations. In particular, the Background of the Invention section of any application may include:

A paragraph(s) describing to the extent practical the state of the prior art **or other information disclosed known to the applicant**, including references to specific prior art or other information where appropriate.⁷⁷ (Emphasis added by Appellants' representative)

No admission has been made that any statements in the Background of the Invention section of the instant application is prior art. No evidence has been provided by the Examiner that any statement in the Background of the Invention section of the instant application qualifies as prior art. No evidence has been provided by the Examiner that any admission has been made by the Appellants. Therefore, the Examiner has failed to establish that the sentences relied upon for the 35 U.S.C. §103(a) rejection are prior art. Writing sentences in the Background of the Invention section of an application does not automatically imply that the sentences are admissions of prior art. As such, the Examiner has failed to establish a *prima facie* case of obviousness for lack of evidence that the prior art references teach or suggest all of the claim limitations.

The Examiner has failed to establish a *prima facie* case of obviousness for lack of clear and particular motivation to combine the Background of the Invention section of the instant application with the teachings of Kablanian et al. In particular, (i) no evidence of a reasonable expectation of success has been provided and (ii) the asserted motivation is a conclusory statement. As such, the claimed invention is fully patentable over the proposed combination and the rejections should be reversed.

The proposed combination appears to add external software for optimizing redundant memory lines and fuse/anti-fuse equipment taught by Kablanian et al. to manual procedures and conventional methods disclosed in the Background of the Invention section. The Examiner has not provided any evidence regarding a reasonable expectation for success of the proposed combination.

⁷⁷ M.P.E.P., Eighth Edition, Revised February 2003, §608.01(c).
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Therefore, a *prima facie* case for obviousness has not been established for lack of clear and particular evidence of a reasonable expectation of success.

Furthermore, the asserted motivation to “determine the optimal utilization”⁷⁸ is a conclusory statement taken out of context. The Background of the Invention section discusses enumeration of fuse locations and verification of a repair using the fuses. In contrast, the full context provided by Kablanian et al. for “optimal utilization” applies to redundant memory lines used to repair defective memory lines. The Background of the Invention section makes no references to memory lines or optimization. Therefore, there is no clear and particular motivation why one of ordinary skill in the art working on fuse enumeration and repair verification would seek a memory line optimization reference such as Kablanian et al. The fact that references can be combined is not sufficient to establish obviousness.⁷⁹ Therefore, the Examiner has failed to establish a *prima facie* case of obviousness for lack of (i) evidence for a reasonable expectation of success and (ii) evidence of motivation to combine or modify the references.

Claims 18 and 19, through dependencies from claim 12, provide a second circuit configured to perform a simulation of the design with at least one of a plurality of fuses programmed for a repair of the design to verify a repair. Assuming, *arguendo*, that the proposed combination of the Background of the Invention and Kablanian et al. would have been obvious (for which the Appellants’ representative does not necessarily agree), the proposed combination still does not teach every element of the pending claims. Despite the Examiner’s suggestion⁸⁰, Kablanian et al. do not

⁷⁸ Office Action, January 10, 2003, page 9, item 56.

⁷⁹ M.P.E.P., Eighth Edition, Revised February 2003, §2143.01.

⁸⁰ Office Action, January 10, 2003, page 9, item 55.

teach or suggest simulating a design with at least one fuse programmed for a repair to verify the repair. **Determining** an optimum utilization of redundant memory lines to repair defective memory lines takes place **before** the repair is performed. In contrast, the claim provides **verifying** the repair **after** simulating the repair.

Furthermore, the Examiner has interpreted the “external software” taught by Kablanian et al. to include simulation software that simulates the repair.⁸¹ However, the Examiner appears to have used the claim language as a template to change the plain meaning of Kablanian et al. Nothing in Kablanian et al. teaches or suggests that the external software performs a simulation of the memory circuit or performs a simulation of a repair to the memory circuit. External software is also not a circuit as per the claim. In contrast, Kablanian et al. teach repairing an actual chip using a conventional laser beam and then retesting the actual chip with automatic test equipment (ATE).⁸² Using a conventional laser and ATE does not teach or suggest simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair as presently claimed. Therefore, the proposed combination does not teach or suggest every element as presently claimed and the rejection should be reversed.

The Examiner has failed to establish a *prima facie* case for obviousness because the proposed combination of the Background of the Invention section and Kablanian et al. do not provide clear and particular evidence of a teaching or suggestion for the claimed data for each of a plurality of fuses. In particular, the rational for the claim rejections make conflicting statements

⁸¹ Advisory Action, March 24, 2003, page 2, item 13.

⁸² Kablanian et al., column 2, lines 7-14.

within the final Office Action regarding two sentences in the Background of the Invention section which read:

The conventional methods to manually associate the fuse path to the fuse locations, or vise versa, use a layout versus schematic (LVS) cross-probe user-interface. Conventional verilog simulation paths are derived by manual translation of schematic paths aided by visual inspection of a netlist.⁸³

Claims 18 and 19, through dependencies from claim 12, provide compiling data for each of a plurality of fuses, wherein the data comprises simulation path data. The Examiner has asserted that the two sentences in the Background of the Invention section teach compiling data for each one of a plurality of fuses, wherein the data comprises **simulation path data**.⁸⁴ In addition, the Examiner has also asserted that the same two sentences teach that the data comprises **schematic path data**.⁸⁵ Furthermore, the Examiner has asserted that the same two sentences teach that the data comprises **physical layout data**.⁸⁶ The same two sentences cannot teach or suggest three different types of data simultaneously. Therefore, no clear and particular evidence has been provided that the Background of the Invention section teaches or suggests compiling data for each of a plurality of fuses, wherein the data comprises simulation path data as presently claimed. As such, the Examiner has failed to establish a *prima facie* case for obviousness due to conflicting interpretations of the Background of the Invention section.

Furthermore, the Examiner has provided conflicting statements regarding the alleged structure taught by the two sentences in the Background of the Invention section. In particular, the

⁸³ Application, page 1, lines 16-20.

⁸⁴ Office Action, January 10, 2003, page 9, item 52.

⁸⁵ Office Action, January 10, 2003, page 15, item 103.

⁸⁶ Office Action, January 10, 2003, page 15, item 106.

Examiner has asserted that the two sentences teach a structure that provides an elevation of the fuses at least one level of abstraction in a design.⁸⁷ However, the Examiner has also asserted that the same two sentences teach a structure that collects data relevant to the fuses that are grouped.⁸⁸ Since the same sentences cannot have two different meanings, the Examiner has failed to provide clear and particular evidence that the Background of the Invention section teaches or suggests every claimed element. As such, the Examiner has failed to establish a *prima facie* case for obviousness due to conflicting interpretations of the Background of the Invention section.

The Examiner has failed to establish a *prima facie* case for obviousness for lack of evidence for every element of the claim. Claims 18 and 19, through dependencies from claim 12, provide a first circuit and a second circuit. No evidence was provided by the Examiner that the references teach or suggest a first circuit or a second circuit as presently claimed.⁸⁹ Therefore, the Examiner has failed to establish that the Background of the Invention section and Kablanian et al. alone, or in combination, teach or suggest every element as presently claimed.

In summary, a *prima facie* case for obviousness has not been established to combine the Background of the Invention section of the instant application and Kablanian et al. No admission has been made that the Background of the Invention section is prior art. No evidence has been provided by the Examiner that the cited sentences in the Background of the Invention section qualify as prior art. The Examiner has not provided clear and particular evidence of motivation to combine the Background of the Invention section with Kablanian et al. Furthermore, the Examiner has made

⁸⁷ Office Action, January 10, 2003, page 16, item 116.

⁸⁸ Office Action, January 10, 2003, page 16, item 119.

⁸⁹ Office Action, January 10, 2003, page 14, item 98.

multiple conflicting interpretations regarding two sentences from the Background of the Invention section relied upon in the rejections. Even if the Background of the Invention section was prior art and the proposed combination were made, the proposed combination still does not teach or suggest (i) a first circuit, (ii) a second circuit and (iii) simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair as presently claimed. As such, the claimed invention is fully patentable over the cited references and the rejections should be reversed.

7. Group 4 (claims 2 and 3) is patentable over the Background of the Invention section in view of Kablanian et al. and Tzori.

The final Office Action does not explicitly include the Tzori reference in the rejection of claim 3.⁹⁰ However, the arguments made by the Examiner against claim 3 reference Tzori.⁹¹ Therefore, Appellants treat claim 3 has being rejected under the Background of the Invention section in view of Kablanian et al. and Tzori.

The Examiner has failed to establish a *prima facie* case for obviousness to combine the Background of the Invention section of the instant application with Kablanian et al. and Tzori. No admission has been made and no evidence has been provided that the Background of the Invention section is prior art. The Examiner has not provided clear and particular evidence of motivation to combine the Background of the Invention section with Kablanian et al. The Examiner has not provided clear and particular evidence of motivation to combine the Background of the Invention section with Kablanian et al. and Tzori. Furthermore, conflicting interpretations regarding

⁹⁰ Office Action, January 10, 2003, page 10, item 62.

⁹¹ Office Action, January 10, 2003, page 10, item 65.

two sentences from the Background of the Invention section exist in the final Office Action. Even if the proposed combination was made, the proposed combination still does not teach or suggest simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair. As such, the claimed invention is fully patentable over the cited references and the rejections should be reversed.

The Examiner has failed to establish a *prima facie* case of obviousness for lack of evidence that the prior art references teach or suggest all of the claim limitations. In particular, the Background of the Invention section of any application may include:

A paragraph(s) describing to the extent practical the state of the prior art **or other information disclosed known to the applicant**, including references to specific prior art or other information where appropriate.⁹² (Emphasis added by Appellants' representative)

No admission has been made that any statements in the Background of the Invention section of the instant application is prior art. No evidence has been provided by the Examiner that any statement in the Background of the Invention section of the instant application qualifies as prior art. No evidence has been provided by the Examiner that any admission has been made by the Appellants. Therefore, the Examiner has failed to establish that the sentences relied upon for the 35 U.S.C. §103(a) rejection are prior art. Writing sentences in the Background of the Invention section of an application does not automatically imply that the sentences are admissions of prior art. As such, the Examiner has failed to establish a *prima facie* case of obviousness for lack of evidence that the prior art references teach or suggest all of the claim limitations.

The Examiner has failed to establish a *prima facie* case of obviousness for lack of clear and particular motivation to combine the Background of the Invention section of the instant

⁹² M.P.E.P., Eighth Edition, Revised February 2003, §608.01(c).
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application with Kablanian et al. In particular, (i) no evidence of a reasonable expectation of success has been provided and (ii) the asserted motivation is a conclusory statement. As such, the claimed invention is fully patentable over the proposed combination and the rejections should be reversed.

The proposed combination appears to add external software for optimizing redundant memory lines and fuse/anti-fuse equipment taught by Kablanian et al. to manual procedures and conventional methods disclosed in the Background of the Invention section. The Examiner has not provided any evidence regarding a reasonable expectation for success of the proposed combination. Therefore, a *prima facie* case for obviousness has not been established for lack of clear and particular evidence of a reasonable expectation of success.

Furthermore, the asserted motivation to “determine the optimal utilization”⁹³ is a conclusory statement taken out of context. The Background of the Invention section discusses enumeration of fuse locations and verification of a repair using the fuses. In contrast, the full context provided by Kablanian et al. for “optimal utilization” applies to redundant memory lines used to repair defective memory lines. The Background of the Invention section makes no references to memory lines or optimization. Therefore, there is no clear and particular motivation why one of ordinary skill in the art working on fuse enumeration and repair verification would seek a memory line optimization reference such as Kablanian et al. The fact that references can be combined is not sufficient to establish obviousness.⁹⁴ Therefore, the Examiner has failed to establish a *prima facie* case of obviousness for lack of (i) evidence for a reasonable expectation of success and (ii) evidence of motivation to combine or modify the references.

⁹³ Office Action, January 10, 2003, page 9, item 56.

⁹⁴ M.P.E.P., Eighth Edition, Revised February 2003, §2143.01.
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The Examiner has failed to establish a *prima facie* case of obviousness for lack of clear and particular motivation to combine the Background of the Invention section of the instant application and Kablanian et al. with Tzori. In particular, (i) no evidence of a reasonable expectation of success has been provided and (ii) the asserted motivation is a conclusory statement. As such, the claimed invention is fully patentable over the proposed combination and the rejections should be reversed.

The Examiner has not provided any evidence regarding a reasonable expectation for success of the proposed combination. Therefore, a *prima facie* case for obviousness has not been established for lack of clear and particular evidence of a reasonable expectation of success.

Furthermore, the asserted motivation, “Since in almost all instances IC manufacturers simulate their designs before fabricating even a prototype” is a conclusory statement.⁹⁵ The Examiner has already asserted that Kablanian et al. teaches simulating the design.⁹⁶ No clear and particular evidence has been provided why one of ordinary skill in the art already simulating a design would be motivated to seek another reference for the sake of simulating the design. Furthermore, the broad statement that almost all IC manufacturers simulate designs does not explain why one or ordinary skill in the art would be motivated to make the specific combination of the Background of the Invention section and Kablanian et al. with Tzori. The fact that references can be combined is not sufficient to establish obviousness.⁹⁷ Therefore, the Examiner has failed to establish a *prima*

⁹⁵ Office Action, January 10, 2003, page 10, items 61 and 66.

⁹⁶ Office Action, January 10, 2003, page 9, item 55.

⁹⁷ M.P.E.P., Eighth Edition, Revised February 2003, §2143.01.

facie case of obviousness for lack of (i) evidence for a reasonable expectation of success and (ii) evidence of motivation to combine or modify the references.

Claims 2 and 3, by dependency from claim 1, provide simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair. Assuming, *arguendo*, that the proposed combination of the Background of the Invention, Kablanian et al. and Tzori would have been obvious (for which the Appellants' representative does not necessarily agree), the proposed combination still does not teach every element of the pending claims. Despite the Examiner's suggestion⁹⁸, Kablanian et al. do not teach or suggest simulating a design with at least one fuse programmed for a repair to verify the repair. **Determining** an optimum utilization of redundant memory lines to repair defective memory lines takes place **before** the repair is performed. In contrast, the claim provides **verifying** the repair **after** simulating the repair.

Furthermore, the Examiner has interpreted the "external software" taught by Kablanian et al. to include simulation software that simulates the repair.⁹⁹ However, the Examiner appears to have used the claim language as a template to change the plain meaning of Kablanian et al. Nothing in Kablanian et al. teaches or suggests that the external software performs a simulation of the memory circuit or performs a simulation of a repair to the memory circuit. In contrast, Kablanian et al. teach repairing an actual chip using a conventional laser beam and then retesting the actual chip with automatic test equipment (ATE).¹⁰⁰ Using a conventional laser and ATE does not teach or suggest simulating a design with at least one of a plurality of fuses programmed for a repair

⁹⁸ Office Action, January 10, 2003, page 9, item 55.

⁹⁹ Advisory Action, March 24, 2003, page 2, item 13.

¹⁰⁰ Kablanian et al., column 2, lines 7-14.

to verify the repair as presently claimed. Therefore, the proposed combination does not teach or suggest every element as presently claimed and the rejections should be reversed.

The Examiner has failed to establish a *prima facie* case for obviousness because the proposed combination of the Background of the Invention section, Kablanian et al. and Tzori do not provide clear and particular evidence of a teaching or suggestion for the claimed data for each of a plurality of fuses. In particular, the rationale for the claim rejections make conflicting statements within the final Office Action regarding two sentences in the Background of the Invention section which read:

The conventional methods to manually associate the fuse path to the fuse locations, or vice versa, use a layout versus schematic (LVS) cross-probe user-interface. Conventional verilog simulation paths are derived by manual translation of schematic paths aided by visual inspection of a netlist.¹⁰¹

Claims 2 and 3, by dependency from claim 1, provide compiling data for each of a plurality of fuses, wherein the data comprises simulation path data. The Examiner has asserted that the two sentences in the Background of the Invention section teach compiling data for each one of a plurality of fuses, wherein the data comprises **simulation path data**.¹⁰² In addition, the Examiner has also asserted that the same two sentences teach that the data comprises **schematic path data**.¹⁰³ Furthermore, the Examiner has asserted that the same two sentences teach that the data comprises **physical layout data**.¹⁰⁴ The same two sentences cannot teach or suggest three different types of data simultaneously. Therefore, no clear and particular evidence has been provided that the Background

¹⁰¹ Application, page 1, lines 16-20 as originally filed.

¹⁰² Office Action, January 10, 2003, page 9, item 52.

¹⁰³ Office Action, January 10, 2003, page 15, item 103.

¹⁰⁴ Office Action, January 10, 2003, page 15, item 106.

of the Invention section teaches or suggests compiling data for each of a plurality of fuses, wherein the data comprises simulation path data as presently claimed. As such, the Examiner has failed to establish a *prima facie* case for obviousness due to conflicting interpretations of the Background of the Invention section.

In summary, a *prima facie* case for obviousness has not been established to combine the Background of the Invention section of the instant application with Kablanian et al and Tzori. No admission has been made that the Background of the Invention section is prior art. No evidence has been provided by the Examiner that the cited sentences in the Background of the Invention section qualify as prior art. The Examiner has not provided clear and particular evidence of motivation to combine the Background of the Invention section with Kablanian et al. The Examiner has not provided clear and particular evidence to add Tzori to the proposed combination. Furthermore, the Examiner has made conflicting interpretations regarding two sentences from the Background of the Invention section relied upon for the rejections. Even if the Background of the Invention section was prior art and the proposed combination were made, the proposed combination still does not teach or suggest simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair as presently claimed. As such, the claimed invention is fully patentable over the cited references and the rejections should be reversed.

8. Group 5 (claim 4) is patentable over the Background of the Invention section in view of Kablanian et al. and Sample et al.

The Examiner has failed to establish a *prima facie* case for obviousness to combine the Background of the Invention section of the instant application with Kablanian et al. and Sample

et al. No admission has been made and no evidence has been provided that the Background of the Invention section is prior art. The Examiner has not provided clear and particular evidence of motivation to combine the Background of the Invention section with Kablanian et al. The Examiner has not provided clear and particular evidence of motivation to combine the Background of the Invention section and Kablanian et al. with Sample et al. Furthermore, conflicting interpretations regarding two sentences from the Background of the Invention section exist in the final Office Action. Even if the proposed combination was made, the proposed combination still does not teach or suggest simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair. As such, the claimed invention is fully patentable over the cited references and the rejection should be reversed.

The Examiner has failed to establish a *prima facie* case of obviousness for lack of evidence that the prior art references teach or suggest all of the claim limitations. In particular, the Background of the Invention section of any application may include:

A paragraph(s) describing to the extent practical the state of the prior art **or other information disclosed known to the applicant**, including references to specific prior art or other information where appropriate.¹⁰⁵ (Emphasis added by Appellants' representative)

No admission has been made that any statements in the Background of the Invention section of the instant application is prior art. No evidence has been provided by the Examiner that any statement in the Background of the Invention section of the instant application qualifies as prior art. No evidence has been provided by the Examiner that any admission has been made by the Appellants. Therefore, the Examiner has failed to establish that the sentences relied upon for the 35 U.S.C. §103(a) rejection are prior art. Writing sentences in the Background of the Invention section of an

¹⁰⁵ M.P.E.P., Eighth Edition, Revised February 2003, §608.01(c).
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application does not automatically imply that the sentences are admissions of prior art. As such, the Examiner has failed to establish a *prima facie* case of obviousness for lack of evidence that the prior art references teach or suggest all of the claim limitations.

The Examiner has failed to establish a *prima facie* case of obviousness for lack of clear and particular motivation to combine the Background of the Invention section of the instant application with Kablanian et al. In particular, (i) no evidence of a reasonable expectation of success has been provided and (ii) the asserted motivation is a conclusory statement. As such, the claimed invention is fully patentable over the proposed combination and the rejection should be reversed.

The proposed combination appears to add external software for optimizing redundant memory lines and fuse/anti-fuse equipment taught by Kablanian et al. to manual procedures and conventional methods disclosed in the Background of the Invention section. The Examiner has not provided any evidence regarding a reasonable expectation for success of the proposed combination. Therefore, a *prima facie* case for obviousness has not been established for lack of clear and particular evidence of a reasonable expectation of success.

Furthermore, the asserted motivation to “determine the optimal utilization”¹⁰⁶ is a conclusory statement taken out of context. The Background of the Invention section discusses enumeration of fuse locations and verification of a repair using the fuses. In contrast, the full context provided by Kablanian et al. for “optimal utilization” applies to redundant memory lines used to repair defective memory lines. The Background of the Invention section makes no references to memory lines or optimization. Therefore, there is no clear and particular motivation why one of ordinary skill in the art working on fuse enumeration and repair verification would seek a memory

¹⁰⁶ Office Action, January 10, 2003, page 9, item 56.
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line optimization reference such as Kablanian et al. The fact that references can be combined is not sufficient to establish obviousness.¹⁰⁷ Therefore, the Examiner has failed to establish a *prima facie* case of obviousness for lack of (i) evidence for a reasonable expectation of success and (ii) evidence of motivation to combine or modify the references.

The Examiner has failed to establish a *prima facie* case of obviousness for lack of clear and particular motivation to combine the Background of the Invention section of the instant application and Kablanian et al. with Sample et al. In particular, (i) no evidence of a reasonable expectation of success has been provided and (ii) the asserted motivation is a conclusory statement. As such, the claimed invention is fully patentable over the proposed combination and the rejection should be reversed.

The Examiner has not provided any evidence regarding a reasonable expectation for success of the proposed combination. Therefore, a *prima facie* case for obviousness has not been established for lack of clear and particular evidence of a reasonable expectation of success.

Furthermore, the asserted motivation that “the transistor list or layout specification is used to bum [sic] fuses” is a conclusory statement.¹⁰⁸ The Examiner has already asserted that Kablanian et al. teaches fuse and/or antifuse equipment for severing circuit fuses.¹⁰⁹ No clear and particular evidence has been provided why one of ordinary skill in the art already burning fuses would be motivated to seek another reference for the sake of burning fuses. Furthermore, the Background of the Invention section concerns enumeration of fuse locations and verification of

¹⁰⁷ M.P.E.P., Eighth Edition, Revised February 2003, §2143.01.

¹⁰⁸ Office Action, January 10, 2003, page 10, items 61 and 66.

¹⁰⁹ Office Action, January 10, 2003, page 9, item 55.

repair using a simulation. In contrast, Sample et al. teach burning fuses in an actual device. No clear and particular evidence has been provided why one of ordinary skill in the art working with fuse locations and repair verification through simulation would be motivated to seek a reference that teaches how to program a real integrated circuit. The fact that references can be combined is not sufficient to establish obviousness.¹¹⁰ Therefore, the Examiner has failed to establish a *prima facie* case of obviousness for lack of (i) evidence for a reasonable expectation of success and (ii) evidence of motivation to combine or modify the references.

Claim 4, by dependency from claim 1, provides simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair. Assuming, *arguendo*, that the proposed combination of the Background of the Invention with Kablanian et al. and Sample et al. would have been obvious (for which the Appellants' representative does not necessarily agree), the proposed combination still does not teach every element of the pending claims. Despite the Examiner's suggestion¹¹¹, Kablanian et al. do not teach or suggest simulating a design with at least one fuse programmed for a repair to verify the repair. **Determining** an optimum utilization of redundant memory lines to repair defective memory lines takes place **before** the repair is performed. In contrast, the claim provides **verifying** the repair **after** simulating the repair.

Furthermore, the Examiner has interpreted the "external software" taught by Kablanian et al. to include simulation software that simulates the repair.¹¹² However, the Examiner appears to have used the claim language as a template to change the plain meaning of Kablanian et

¹¹⁰ M.P.E.P., Eighth Edition, Revised February 2003, §2143.01.

¹¹¹ Office Action, January 10, 2003, page 9, item 55.

¹¹² Advisory Action, March 24, 2003, page 2, item 13.

al. Nothing in Kablanian et al. teaches or suggests that the external software performs a simulation of the memory circuit or performs a simulation of a repair to the memory circuit. In contrast, Kablanian et al. teach repairing an actual chip using a conventional laser beam and then retesting the actual chip with automatic test equipment (ATE).¹¹³ Using a conventional laser and ATE does not teach or suggest simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair as presently claimed. Therefore, the proposed combination does not teach or suggest every element as presently claimed and the rejection should be reversed.

The Examiner has failed to establish a *prima facie* case for obviousness because the proposed combination of the Background of the Invention section with Kablanian et al. and Sample et al. do not provide clear and particular evidence of a teaching or suggestion for the claimed data for each of a plurality of fuses. In particular, the rationale for the claim rejection makes conflicting statements within the final Office Action regarding two sentences in the Background of the Invention section which read:

The conventional methods to manually associate the fuse path to the fuse locations, or vise versa, use a layout versus schematic (LVS) cross-probe user-interface. Conventional verilog simulation paths are derived by manual translation of schematic paths aided by visual inspection of a netlist.¹¹⁴

Claim 4, by dependency from claim 1, provides compiling data for each of a plurality of fuses, wherein the data comprises simulation path data. The Examiner has asserted that the two sentences in the Background of the Invention section teach compiling data for each one of a plurality of fuses, wherein the data comprises **simulation path data**.¹¹⁵ In addition, the Examiner has also asserted that

¹¹³ Kablanian et al., column 2, lines 7-14.

¹¹⁴ Application, page 1, lines 16-20.

¹¹⁵ Office Action, January 10, 2003, page 9, item 52.

the same two sentences teach that the data comprises **schematic path data**.¹¹⁶ Furthermore, the Examiner has asserted that the same two sentences teach that the data comprises **physical layout data**.¹¹⁷ The same two sentences cannot teach or suggest three different types of data simultaneously. Therefore, no clear and particular evidence has been provided that the Background of the Invention section teaches or suggests compiling data for each of a plurality of fuses, wherein the data comprises simulation path data as presently claimed. As such, the Examiner has failed to establish a *prima facie* case for obviousness due to conflicting interpretations of the Background of the Invention section.

In summary, a *prima facie* case for obviousness has not been established to combine the Background of the Invention section of the instant application with Kablanian et al. and Sample et al. No admission has been made that the Background of the Invention section is prior art. No evidence has been provided by the Examiner that the cited sentences in the Background of the Invention section qualify as prior art. The Examiner has not provided clear and particular evidence of motivation to combine the Background of the Invention section with Kablanian et al. The Examiner has not provided clear and particular evidence to add Sample et al. to the proposed combination. Furthermore, the Examiner has made conflicting interpretations regarding two sentences from the Background of the Invention section relied upon in the rejection. Even if the Background of the Invention section was prior art and the proposed combination were made, the proposed combination still does not teach or suggest simulating a design with at least one of a

¹¹⁶ Office Action, January 10, 2003, page 15, item 103.

¹¹⁷ Office Action, January 10, 2003, page 15, item 106.

plurality of fuses programmed for a repair to verify the repair as presently claimed. As such, the claimed invention is fully patentable over the cited references and the rejection should be reversed.

9. Group 8 (claims 8, 10 and 11) is patentable over the Background of the Invention section in view of Kablanian et al. and Higgins et al.

The Examiner has failed to establish a *prima facie* case for obviousness to combine the Background of the Invention section of the instant application with Kablanian et al. and Higgins et al. No admission has been made and no evidence has been provided that the Background of the Invention section is prior art. The Examiner has not provided clear and particular evidence of motivation to combine the Background of the Invention section with Kablanian et al. The Examiner has not provided clear and particular evidence of motivation to combine the Background of the Invention section and Kablanian et al. with Higgins et al. Furthermore, multiple conflicting interpretations regarding three sentences from the Background of the Invention section exist in the final Office Action. Even if the proposed combination was made, the proposed combination still does not teach or suggest simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair. As such, the claimed invention is fully patentable over the cited references and the rejections should be reversed.

The Examiner has failed to establish a *prima facie* case of obviousness for lack of evidence that the prior art references teach or suggest all of the claim limitations. In particular, the Background of the Invention section of any application may include:

A paragraph(s) describing to the extent practical the state of the prior art **or other information disclosed known to the applicant**, including references to specific prior art or other information where appropriate.¹¹⁸ (Emphasis added by Appellants' representative)

No admission has been made that any statements in the Background of the Invention section of the instant application is prior art. No evidence has been provided by the Examiner that any statement in the Background of the Invention section of the instant application qualifies as prior art. No evidence has been provided by the Examiner that any admission has been made by the Appellants. Therefore, the Examiner has failed to establish that the sentences relied upon for the 35 U.S.C. §103(a) rejection are prior art. Writing sentences in the Background of the Invention section of an application does not automatically imply that the sentences are admissions of prior art. As such, the Examiner has failed to establish a *prima facie* case of obviousness for lack of evidence that the prior art references teach or suggest all of the claim limitations.

The Examiner has failed to establish a *prima facie* case of obviousness for lack of clear and particular motivation to combine the Background of the Invention section of the instant application with Kablanian et al. In particular, (i) no evidence of a reasonable expectation of success has been provided and (ii) the asserted motivation is a conclusory statement. As such, the claimed invention is fully patentable over the proposed combination and the rejections should be reversed.

The proposed combination appears to add external software for optimizing redundant memory lines and fuse/anti-fuse equipment taught by Kablanian et al. to manual procedures and conventional methods disclosed in the Background of the Invention section. The Examiner has not provided any evidence regarding a reasonable expectation for success of the proposed combination.

¹¹⁸ M.P.E.P., Eighth Edition, Revised February 2003, §608.01(c).
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Therefore, a *prima facie* case for obviousness has not been established for lack of clear and particular evidence of a reasonable expectation of success.

Furthermore, the asserted motivation to “determine the optimal utilization”¹¹⁹ is a conclusory statement taken out of context. The Background of the Invention section discusses enumeration of fuse locations and verification of a repair using the fuses. In contrast, the full context provided by Kablanian et al. for “optimal utilization” applies to redundant memory lines used to repair defective memory lines. The Background of the Invention section makes no references to memory lines or optimization. Therefore, there is no clear and particular motivation why one of ordinary skill in the art working on fuse enumeration and repair verification would seek a memory line optimization reference such as Kablanian et al. The fact that references can be combined is not sufficient to establish obviousness.¹²⁰ Therefore, the Examiner has failed to establish a *prima facie* case of obviousness for lack of (i) evidence for a reasonable expectation of success and (ii) evidence of motivation to combine or modify the references.

The Examiner has failed to establish a *prima facie* case of obviousness for lack of clear and particular motivation to combine the Background of the Invention section of the instant application and Kablanian et al. with Higgins et al. In particular, (i) no evidence of a reasonable expectation of success has been provided and (ii) the asserted motivation is a conclusory statement. As such, the claimed invention is fully patentable over the proposed combination and the rejections should be reversed.

¹¹⁹ Office Action, January 10, 2003, page 9, item 56.

¹²⁰ M.P.E.P., Eighth Edition, Revised February 2003, §2143.01.
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The Examiner has not provided any evidence regarding a reasonable expectation for success of the proposed combination. Therefore, a *prima facie* case for obviousness has not been established for lack of clear and particular evidence of a reasonable expectation of success.

Furthermore, the asserted motivation that “repair procedures result in higher yields” is a conclusory statement.¹²¹ The Examiner has already asserted that Kablanian et al. teaches fuse and/or antifuse equipment for severing circuit fuses.¹²² No clear and particular evidence has been provided why one of ordinary skill in the art already burning fuses would be motivated to seek another reference to burn fuses for the sake of a higher yield. Furthermore, the Background of the Invention section concerns enumeration of fuse locations and verification of repair using the fuses. In contrast, Higgins et al. teach burning fuses in actual hardware. No clear and particular evidence has been provided why one of ordinary skill in the art working with fuse locations and repair verification through simulation would be motivated to seek a reference that teaches higher yields using a laser to repair actual hardware. The fact that references can be combined is not sufficient to establish obviousness.¹²³ Therefore, the Examiner has failed to establish a *prima facie* case of obviousness for lack of (i) evidence for a reasonable expectation of success and (ii) evidence of motivation to combine or modify the references.

Claims 8, 10 and 11, by dependency from claim 1, provide simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair. Assuming, *arguendo*, that the proposed combination of the Background of the Invention with Kablanian et al. and Higgins

¹²¹ Office Action, January 10, 2003, page 13, item 84.

¹²² Office Action, January 10, 2003, page 9, item 55.

¹²³ M.P.E.P., Eighth Edition, Revised February 2003, §2143.01.

et al. would have been obvious (for which the Appellants' representative does not necessarily agree), the proposed combination still does not teach every element of the pending claims. Despite the Examiner's suggestion¹²⁴, Kablanian et al. do not teach or suggest simulating a design with at least one fuse programmed for a repair to verify the repair. **Determining** an optimum utilization of redundant memory lines to repair defective memory lines takes place **before** the repair is performed. In contrast, the claim provides **verifying** the repair **after** simulating the repair.

Furthermore, the Examiner has interpreted the "external software" taught by Kablanian et al. to include simulation software that simulates the repair.¹²⁵ However, the Examiner appears to have used the claim language as a template to change the plain meaning of Kablanian et al. Nothing in Kablanian et al. teaches or suggests that the external software performs a simulation of the memory circuit or performs a simulation of a repair to the memory circuit. In contrast, Kablanian et al. teach repairing an actual chip using a conventional laser beam and then retesting the actual chip with automatic test equipment (ATE).¹²⁶ Using a conventional laser and ATE does not teach or suggest simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair as presently claimed. Therefore, the proposed combination does not teach or suggest every element as presently claimed and the rejection should be reversed.

The Examiner has failed to establish a *prima facie* case for obviousness because the proposed combination of the Background of the Invention section with Kablanian et al. and Higgins et al. does not provide clear and particular evidence of a teaching or suggestion for the claimed data

¹²⁴ Office Action, January 10, 2003, page 9, item 55.

¹²⁵ Advisory Action, March 24, 2003, page 2, item 13.

¹²⁶ Kablanian et al., column 2, lines 7-14.

for each of a plurality of fuses. In particular, the rational for the claim rejections make conflicting statements within the final Office Action regarding two sentences in the Background of the Invention section which read:

The conventional methods to manually associate the fuse path to the fuse locations, or vise versa, use a layout versus schematic (LVS) cross-probe user-interface. Conventional verilog simulation paths are derived by manual translation of schematic paths aided by visual inspection of a netlist.¹²⁷

Claims 8, 10 and 11, through dependency from claim 1, provide compiling data for each of a plurality of fuses, wherein the data comprises simulation path data. The Examiner has asserted that the two sentences in the Background of the Invention section teach compiling data for each one of a plurality of fuses, wherein the data comprises **simulation path data**.¹²⁸ In addition, the Examiner has also asserted that the same two sentences teach that the data comprises **schematic path data**.¹²⁹ Furthermore, the Examiner has asserted that the same two sentences teach that the data comprises **physical layout data**.¹³⁰ The same two sentences cannot teach or suggest three different types of data simultaneously. Therefore, no clear and particular evidence has been provided that the Background of the Invention section teaches or suggests compiling data for each of a plurality of fuses, wherein the data comprises simulation path data as presently claimed. As such, the Examiner has failed to establish a *prima facie* case for obviousness due to conflicting interpretations of the Background of the Invention section.

¹²⁷ Application, page 1, lines 16-20 as originally filed.

¹²⁸ Office Action, January 10, 2003, page 9, item 52.

¹²⁹ Office Action, January 10, 2003, page 15, item 103.

¹³⁰ Office Action, January 10, 2003, page 15, item 106.

Furthermore, the Examiner has made conflicting statements regarding another sentence in the Background of the Invention section of the instant application which reads:

Conventional methods exist to manually associate a fuse path to a fuse location or the fuse location to the fuse path, one at a time.¹³¹

The Examiner has asserts that the above sentence teaches **generating a fuse report**.¹³² Examiner has further asserted that the same sentence teaches **listing physical locations** of a device in the design in response to the fuse report.¹³³ The Examiner has asserted that the same sentence teaches **generating a repair file** that predicts at least one of a plurality of fuses programmed for a repair.¹³⁴ Finally, the Examiner has asserted that the same sentence teaches **listing an output of a repair program** as a list of coordinates for at least one of a plurality fuses programmed for a repair in terms of a plurality of logical addresses.¹³⁵ Since the single sentence cannot teach four very different steps, the Examiner has failed to establish clear and particular evidence that the Background of the Invention section, Kablanian et al. and Higgins et al. alone, or in combination, teach or suggest every claim element.

In summary, a *prima facie* case for obviousness has not been established to combine the Background of the Invention section of the instant application with Kablanian et al. and Higgins et al. No admission has been made that the Background of the Invention section is prior art. No evidence has been provided by the Examiner that the cited sentences in the Background of the

¹³¹ Application, page 1, lines 14-15.

¹³² Office Action, January 10, 2003, page 11, item 74.

¹³³ Office Action, January 10, 2003, page 12, item 77.

¹³⁴ Office Action, January 10, 2003, page 12, item 80.

¹³⁵ Office Action, January 10, 2003, page 13, item 91.

Invention section qualify as prior art. The Examiner has not provided clear and particular evidence of motivation to combine the Background of the Invention section with Kablanian et al. and Higgins et al. Furthermore, the Examiner has made multiple conflicting interpretations regarding three sentences from the Background of the Invention section relied upon in the rejections. Even if the Background of the Invention section was prior art and the proposed combination were made, the proposed combination still does not teach or suggest simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair as presently claimed. As such, the claimed invention is fully patentable over the cited references and the rejections should be reversed.

10. Group 9 (claims 9 and 17) is patentable over the Background of the Invention section in view of Kablanian et al., Higgins et al. and Tzori.

The final Office Action does not explicitly include the Higgins et al. reference in the rejection of claim 17.¹³⁶ However, the claim 17 depends from claim 8 for which the Examiner used Higgins et al. in the rejection.¹³⁷ Therefore, Appellants treat claim 17 has being rejected under the Background of the Invention section in view of Kablanian et al., Tzori and Higgins et al.

The Examiner has failed to establish a *prima facie* case for obviousness to combine the Background of the Invention section of the instant application with Kablanian et al., Higgins et al. and Tzori. No admission has been made and no evidence has been provided that the Background of the Invention section is prior art. The Examiner has not provided clear and particular evidence of motivation to combine the Background of the Invention section with Kablanian et al. The

¹³⁶ Office Action, January 10, 2003, page 15, item 110.

¹³⁷ Office Action, January 10, 2003, page 12, item 81.

Examiner has not provided clear and particular evidence of motivation to combine the Background of the Invention section and Kablanian et al. with Higgins et al. The Examiner has not provided clear and particular evidence of motivation to combine the Background of the Invention section, Kablanian et al. and Higgins et al. with Tzori. Furthermore, multiple conflicting interpretations regarding three sentences from the Background of the Invention section exist in the final Office Action. Even if the proposed combination was made, the proposed combination still does not teach or suggest simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair. As such, the claimed invention is fully patentable over the cited references and the rejections should be reversed.

The Examiner has failed to establish a *prima facie* case of obviousness for lack of evidence that the prior art references teach or suggest all of the claim limitations. In particular, the Background of the Invention section of any application may include:

A paragraph(s) describing to the extent practical the state of the prior art **or other information disclosed known to the applicant**, including references to specific prior art or other information where appropriate.¹³⁸ (Emphasis added by Appellants' representative)

No admission has been made that any statements in the Background of the Invention section of the instant application is prior art. No evidence has been provided by the Examiner that any statement in the Background of the Invention section of the instant application qualifies as prior art. No evidence has been provided by the Examiner that any admission has been made by the Appellants. Therefore, the Examiner has failed to establish that the sentences relied upon for the 35 U.S.C. §103(a) rejection are prior art. Writing sentences in the Background of the Invention section of an application does not automatically imply that the sentences are admissions of prior art. As such, the

¹³⁸ M.P.E.P., Eighth Edition, Revised February 2003, §608.01(c).
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Examiner has failed to establish a *prima facie* case of obviousness for lack of evidence that the prior art references teach or suggest all of the claim limitations.

The Examiner has failed to establish a *prima facie* case of obviousness for lack of clear and particular motivation to combine the Background of the Invention section of the instant application with the teachings of Kablanian et al. In particular, (i) no evidence of a reasonable expectation of success has been provided and (ii) the asserted motivation is a conclusory statement. As such, the claimed invention is fully patentable over the proposed combination and the rejections should be reversed.

The proposed combination appears to add external software for optimizing redundant memory lines and fuse/anti-fuse equipment taught by Kablanian et al. to manual procedures and conventional methods disclosed in the Background of the Invention section. The Examiner has not provided any evidence regarding a reasonable expectation for success of the proposed combination. Therefore, a *prima facie* case for obviousness has not been established for lack of clear and particular evidence of a reasonable expectation of success.

Furthermore, the asserted motivation to “determine the optimal utilization”¹³⁹ is a conclusory statement taken out of context. The Background of the Invention section discusses enumeration of fuse locations and verification of a repair using the fuses. In contrast, the full context provided by Kablanian et al. for “optimal utilization” applies to redundant memory lines used to repair defective memory lines. The Background of the Invention section makes no references to memory lines or optimization. Therefore, there is no clear and particular motivation why one of ordinary skill in the art working on fuse enumeration and repair verification would seek a memory

¹³⁹ Office Action, January 10, 2003, page 9, item 56.
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line optimization reference such as Kablanian et al. The fact that references can be combined is not sufficient to establish obviousness.¹⁴⁰ Therefore, the Examiner has failed to establish a *prima facie* case of obviousness for lack of (i) evidence for a reasonable expectation of success and (ii) evidence of motivation to combine or modify the references.

The Examiner has failed to establish a *prima facie* case of obviousness for lack of clear and particular motivation to combine the Background of the Invention section of the instant application and Kablanian et al. with Higgins et al. In particular, (i) no evidence of a reasonable expectation of success has been provided and (ii) the asserted motivation is a conclusory statement. As such, the claimed invention is fully patentable over the proposed combination and the rejections should be reversed.

The Examiner has not provided any evidence regarding a reasonable expectation for success of the proposed combination. Therefore, a *prima facie* case for obviousness has not been established for lack of clear and particular evidence of a reasonable expectation of success.

Furthermore, the asserted motivation that “repair procedures result in higher yields” is a conclusory statement.¹⁴¹ The Examiner has already asserted that Kablanian et al. teaches fuse and/or antifuse equipment for severing circuit fuses.¹⁴² No clear and particular evidence has been provided why one of ordinary skill in the art already burning fuses would be motivated to seek another reference to burn fuses for the sake of a higher yield. Furthermore, the Background of the Invention section concerns enumeration of fuse locations and verification of repair using the fuses.

¹⁴⁰ M.P.E.P., Eighth Edition, Revised February 2003, §2143.01.

¹⁴¹ Office Action, January 10, 2003, page 13, item 84.

¹⁴² Office Action, January 10, 2003, page 9, item 55.

In contrast, Higgins et al. teach burning fuses in actual hardware. No clear and particular evidence has been provided why one of ordinary skill in the art working with fuse locations and repair verification through simulation would be motivated to seek a reference that teaches higher yields using a laser to repair actual hardware. The fact that references can be combined is not sufficient to establish obviousness.¹⁴³ Therefore, the Examiner has failed to establish a *prima facie* case of obviousness for lack of (i) evidence for a reasonable expectation of success and (ii) evidence of motivation to combine or modify the references.

The Examiner has failed to establish a *prima facie* case of obviousness for lack of clear and particular motivation to combine the Background of the Invention section of the instant application and Kablanian et al. and Higgins et al. with Tzori. In particular, (i) no evidence of a reasonable expectation of success has been provided and (ii) the asserted motivation is a conclusory statement. As such, the claimed invention is fully patentable over the proposed combination and the rejections should be reversed.

The Examiner has not provided any evidence regarding a reasonable expectation for success of the proposed combination. Therefore, a *prima facie* case for obviousness has not been established for lack of clear and particular evidence of a reasonable expectation of success.

Furthermore, the asserted motivation, "Since in almost all instances IC manufacturers simulate their designs before fabricating even a prototype" is a conclusory statement.¹⁴⁴ The Examiner has already asserted that Kablanian et al. teaches simulating the design.¹⁴⁵ No clear and

¹⁴³ M.P.E.P., Eighth Edition, Revised February 2003, §2143.01.

¹⁴⁴ Office Action, January 10, 2003, page 13, item 88.

¹⁴⁵ Office Action, January 10, 2003, page 9, item 55.

particular evidence has been provided why one of ordinary skill in the art already simulating a design would be motivated to seek another reference for the sake of simulating the design. Furthermore, the broad statement that almost all IC manufacturers simulate designs does not explain why one of ordinary skill in the art would be motivated to make the specific combination of the Background of the Invention section, Kablanian et al. and Higgins et al. with Tzori. The fact that references can be combined is not sufficient to establish obviousness.¹⁴⁶ Therefore, the Examiner has failed to establish a *prima facie* case of obviousness for lack of (i) evidence for a reasonable expectation of success and (ii) evidence of motivation to combine or modify the references.

Claims 9 and 17, by dependency from claim 1, provide simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair. Assuming, *arguendo*, that the proposed combination of the Background of the Invention with Kablanian et al., Higgins et al. and Tzori would have been obvious (for which the Appellants' representative does not necessarily agree), the proposed combination still does not teach every element of the pending claims. Despite the Examiner's suggestion¹⁴⁷, Kablanian et al. do not teach or suggest simulating a design with at least one fuse programmed for a repair to verify the repair. **Determining** an optimum utilization of redundant memory lines to repair defective memory lines takes place **before** the repair is performed. In contrast, the claim provides **verifying** the repair **after** simulating the repair.

Furthermore, the Examiner has interpreted the "external software" taught by Kablanian et al. to include simulation software that simulates the repair.¹⁴⁸ However, the Examiner

¹⁴⁶ M.P.E.P., Eighth Edition, Revised February 2003, §2143.01.

¹⁴⁷ Office Action, January 10, 2003, page 9, item 55.

¹⁴⁸ Advisory Action, March 24, 2003, page 2, item 13.

appears to have used the claim language as a template to change the plain meaning of Kablanian et al. Nothing in Kablanian et al. teaches or suggests that the external software performs a simulation of the memory circuit or performs a simulation of a repair to the memory circuit. In contrast, Kablanian et al. teach repairing an actual chip using a conventional laser beam and then retesting the actual chip with automatic test equipment (ATE).¹⁴⁹ Using a conventional laser and ATE does not teach or suggest simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair as presently claimed. Therefore, the proposed combination does not teach or suggest every element as presently claimed and the rejections should be reversed.

The Examiner has failed to establish a *prima facie* case for obviousness because the proposed combination of the Background of the Invention section with Kablanian et al., Higgins et al. and Tzori does not provide clear and particular evidence of a teaching or suggestion for the claimed data for each of a plurality of fuses. In particular, the rationale for the claim rejections make conflicting statements within the final Office Action regarding two sentences in the Background of the Invention section which read:

The conventional methods to manually associate the fuse path to the fuse locations, or vice versa, use a layout versus schematic (LVS) cross-probe user-interface. Conventional verilog simulation paths are derived by manual translation of schematic paths aided by visual inspection of a netlist.¹⁵⁰

Claims 9 and 17, through dependency from claim 1, provide compiling data for each of a plurality of fuses, wherein the data comprises simulation path data. The Examiner has asserted that the two sentences in the Background of the Invention section teach compiling data for each one of a plurality

¹⁴⁹ Kablanian et al., column 2, lines 7-14.

¹⁵⁰ Application, page 1, lines 16-20.

of fuses, wherein the data comprises **simulation path data**.¹⁵¹ In addition, the Examiner has also asserted that the same two sentences teach that the data comprises **schematic path data**.¹⁵² Furthermore, the Examiner has asserted that the same two sentences teach that the data comprises **physical layout data**.¹⁵³ The same two sentences cannot teach or suggest three different types of data simultaneously. Therefore, no clear and particular evidence has been provided that the Background of the Invention section teaches or suggests compiling data for each of a plurality of fuses, wherein the data comprises simulation path data as presently claimed. As such, the Examiner has failed to establish a *prima facie* case for obviousness due to conflicting interpretations of the Background of the Invention section.

Furthermore, the Examiner has made conflicting statements regarding another sentence in the Background of the Invention section of the instant application which reads:

Conventional methods exist to manually associate a fuse path to a fuse location or the fuse location to the fuse path, one at a time.¹⁵⁴

The Examiner has asserts that the above sentence teaches **generating a fuse report**.¹⁵⁵ Examiner has further asserted that the same sentence teaches **listing physical locations** of a device in the design in response to the fuse report.¹⁵⁶ The Examiner has asserted that the same sentence teaches

¹⁵¹ Office Action, January 10, 2003, page 9, item 52.

¹⁵² Office Action, January 10, 2003, page 15, item 103.

¹⁵³ Office Action, January 10, 2003, page 15, item 106.

¹⁵⁴ Application, page 1, lines 14-15 as originally filed.

¹⁵⁵ Office Action, January 10, 2003, page 11, item 74.

¹⁵⁶ Office Action, January 10, 2003, page 12, item 77.

generating a repair file that predicts at least one of a plurality of fuses programmed for a repair.¹⁵⁷

Finally, the Examiner has asserted that the same sentence teaches **listing an output of a repair program** as a list of coordinates for at least one of a plurality fuses programmed for a repair in terms of a plurality of logical addresses.¹⁵⁸ Since the single sentence cannot teach four very different steps, the Examiner has failed to establish clear and particular evidence that the Background of the Invention section, Kablanian et al., Higgins et al. and Tzori alone, or in combination, teach or suggest every claim element.

In summary, a *prima facie* case for obviousness has not been established to combine the Background of the Invention section of the instant application with Kablanian et al., Higgins et al. and Tzori. No admission has been made that the Background of the Invention section is prior art. No evidence has been provided by the Examiner that the cited sentences in the Background of the Invention section qualify as prior art. The Examiner has not provided clear and particular evidence of motivation to combine the Background of the Invention section with Kablanian et al. and Higgins et al. The Examiner has not provided clear and particular evidence of motivation to combine the Background of the Invention section with Kablanian et al., Higgins et al. and Tzori. Furthermore, the Examiner has made multiple conflicting interpretations regarding three sentences from the Background of the Invention section relied upon in the rejections. Even if the Background of the Invention section was prior art and the proposed combination were made, the proposed combination still does not teach or suggest simulating a design with at least one of a plurality of fuses

¹⁵⁷ Office Action, January 10, 2003, page 12, item 80.

¹⁵⁸ Office Action, January 10, 2003, page 13, item 91.

programmed for a repair to verify the repair as presently claimed. As such, the claimed invention is fully patentable over the cited references and the rejections should be reversed.

Groups 1-10 are separately patentable.

During prosecution, each independent and dependent claim is considered to be separately patentable over every other claim.¹⁵⁹ As such, each of the above groups is considered to be separately patentable over every other group.¹⁶⁰ In particular, each of the groups includes a unique combination of arguments that allow individual groups to stand over the references even if all of the other groups fall.

Each of groups 1-10 includes arguments that there is no motivation to combine the Background of the Invention section with Kablanian et al. Group 2 includes an argument that a first structure has not been taught or suggested. Since group 1 does not depend on the first structure argument, group 2 may be found patentable even if group 1 is not.

Group 3 includes an argument that a second structure has not been taught or suggested. Since groups 1-2 do not depend upon the second structure argument, group 3 may be found patentable even if groups 1 and/or 2 are not.

Group 4 includes an argument that there is no motivation to combine Tzori with the Background of the Invention section and Kablanian et al. Since groups 1-3 do not depend upon the Tzori argument, group 4 may be found patentable even if groups 1, 2 and/or 3 are not.

¹⁵⁹ See, e.g., *Rowe v. Dror*, 42 USPQ2d 1550, 1552 (Fed. Cir. 1997), *Preemption Devices, Inc. v. Minnesota Mining and Manufacturing Company*, 221 USPQ 841, 843 (Fed. Cir. 1984), and *Jones v. Hardy*, 727 F.2d 1524, 1528, 220 USPQ 1021, 1024 (Fed. Cir. 1984) (It is well established that each claim in a patent constitutes a separate invention.).

¹⁶⁰ Manual of Patent Examining Procedure (M.P.E.P.), Eighth Edition, August, 2001, §1206.
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Group 5 includes an argument that there is no motivation to combine Sample et al. with the Background of the Invention section and Kablanian et al. Since groups 1-4 do not depend upon the Sample et al. argument, group 5 may be found patentable even if groups 1, 2, 3 and/or 4 are not.

Group 6 includes an argument that no clear and particular evidence has been established for interpreting a cited sentence from the Background of the Invention section. Since groups 1-5 do not depend upon the interpretation argument, group 6 may be found patentable even if groups 1, 2, 3, 4 and/or 5 are not.

Group 7 includes an argument that no clear and particular evidence has been established for interpreting a cited sentence from the Background of the Invention section. Since groups 1-5 do not depend upon the argument, group 7 may be found patentable even if groups 1, 2, 3, 4 and/or 5 are not. Group 7 includes an arguments for definiteness. Since group 6 does not depend upon the definiteness argument, group 6 may be found patentable even if group 7 is not.

Group 8 includes an argument that there is no motivation to combine Higgins et al. with the Background of the Invention section and Kablanian et al. Since groups 1-7 do not depend upon the Higgins et al. argument, group 8 may be found patentable even if groups 1, 2, 3, 4, 5, 6 and/or 7 are not.

Group 9 includes an argument that there is no motivation to combine Higgins et al. and Tzori with the Background of the Invention section and Kablanian et al. Since groups 1-8 do not depend on both the Higgins et al. and the Tzori arguments, group 9 may be found patentable even if groups 1, 2, 3, 4, 5, 6, 7 and/or 8 are not.

Group 10 includes an argument that there is no clear and particular evidence for a structure alleged to be taught in the Background of the Invention section. Since groups 1-9 do not depend on the argument, group 10 may be found patentable even if groups 1, 2, 3, 4, 5, 6, 7, 8 and/or 9 are not.

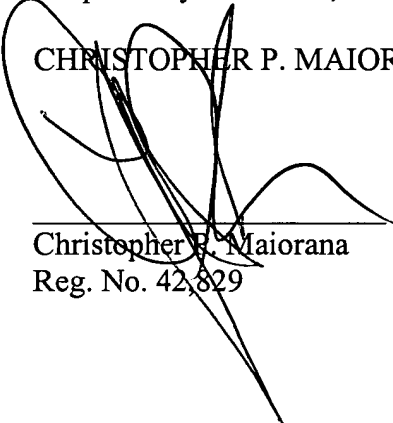
C. CONCLUSION

None of the cited references suggest simulating a design with at least one of a plurality of fuses programmed for a repair to verify the repair as recited in independent claims 1, 12 and 13. No admission has been made that the Background of the Invention section of the instant application is prior art. No evidence has been provided by the Examiner that the Background of the Invention section is prior art or that there has been an admission. Furthermore, a *prima facie* case for obviousness has not been established to combine the Background of the Invention section with Kablanian et al., Tzori, Sample et al. and/or Higgins et al. Hence, the Examiner has clearly erred with respect to the patentability of the claimed invention. It is respectfully requested that the Board

overturn the Examiner's rejection of all pending claims, and hold that the claims are not rendered obvious by the cited reference. However, should the Board find the arguments herein in support of independent claims 1, 12, and/or 13 unpersuasive, the Board is respectfully requested to carefully consider the arguments set forth above in support of each of the independently patentable groups.

Respectfully submitted,

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IX. APPENDIX

The claims of the present application which are involved in this appeal are as follows:

- 1 1. A method of verifying a repair of a design, comprising the steps of:
 - 2 (A) generating an enumeration of a plurality of fuses in said design;
 - 3 (B) compiling data for each of said fuses, wherein said data comprises simulation
4 path data; and
 - 5 (C) simulating said design with at least one of said fuses programmed for said
6 repair to verify said repair.
- 1 2. The method according to claim 1, wherein said simulation path data comprises
2 verilog simulation path data.
- 1 3. The method according to claim 14, wherein said schematic path data
2 comprises at least one of a schematic path, a property, a hierarchy and a verilog path .
- 1 4. The method according to claim 1, wherein step (B) further comprises the sub-
2 step of:
3 generating a list of layout coordinates and paths in said design as part of said
4 compiling.
- 1 5. The method according to claim 1, further comprising the step of:
2 generating a fuse report.

1 6. The method according to claim 5, further comprising the step of:
2 listing physical locations of a device in said design in response to said fuse report.

1 7. The method according to claim 1, further comprising the step of:
2 generating a repair file that predicts said at least one of said fuses programmed for
3 said repair.

1 8. The method according to claim 7, further comprising the step of:
2 creating a repair program in response to said repair file.

1 9. The method according to claim 8, further comprising the step of:
2 verifying a function of said design in response to said repair program.

1 10. The method according to claim 8, further comprising the step of:
2 listing an output of said repair program as a list of coordinates for said at least one
3 of said fuses programmed for said repair in terms of a plurality of logical addresses.

1 11. The method according to claim 10, further comprising the step of:
2 storing said coordinates in a memory.

1 12. An apparatus comprising:
2 a first circuit configured to enumerate a plurality of fuses in a design; and
3 a second circuit configured to (i) compile data for each of said fuses, wherein said

data comprises simulation path data and (ii) perform a simulation said design with at least one of said fuses programmed for a repair of said design to verify said repair.

13. An apparatus comprising:
means for generating an enumeration of a plurality of fuses in a design;
means for compiling data for each of said fuses, wherein said data comprises simulation path data; and
means for simulating said design with at least one of said fuses programmed for a repair of said design to verify said repair.

14. The method according to claim 1, wherein said data further comprises schematic path data.

15. The method according to claim 1, wherein said data further comprises physical location data.

16. The method according to claim 1, further comprising the step of:
mapping a plurality of co-ordinates of said fuses to a plurality of verilog program statements.

17. The method according to claim 8, further comprising the step of:
checking said repair file and said repair program for an error.

1 18. The apparatus according to claim 12, wherein said first circuit is further
2 configured to provide an elevation of said fuses at least one level of abstraction in said design.

1 19. The apparatus according to claim 12, wherein said first circuit is further
2 configured to collect data relevant to said fuses that are grouped.

1 20. The apparatus according to claim 12, wherein said second circuit is further
2 configured to write a report file.